MASTER THESIS PHYSICS

Characterization of Compressed Baryonic Matter Silicon Tracking Systems detector modules

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Dachi Okropiridze

March, 2023

Declaration of independence

I, Dachi Okropiridze, declare that this Master's thesis is my own original work and that I have fully acknowledged all sources of information that I have used in my research. The research presented in this thesis has not been submitted in whole or in part for any other academic degree or qualification. All data and results presented in this thesis are accurate to the best of my knowledge and have not been manipulated or falsified in any way. I understand that any breach of academic integrity may result in the revocation of my degree.

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Abstract

In this work, a set of experiments have been conducted at the Gesellschaft fur Schwerionenforschung GmbH (GSI) Facility for Antiproton and Ion Research (FAIR) facility by Master student Dachi Okropiridze at the Free University of Berlin. Tests were conducted to characterize the Silicon Tracking Systems (STS) detector modules for the Compressed Baryonic Matter (CBM) experiment, which aims to examine the QCD phase diagram in regions of high baryon densities. The STS is a crucial detector for the CBM experiment, and the purpose of these experiments was to examine the characteristics of the STS modules under varying temperatures. Experiments included testing sensors at various operating temperatures, characterizing their physical properties, and conducting noise studies on STS modules. In addition, Cold Start-Up Cycling or Low-temperature power cycling was conducted to investigate the thermal effects of low temperatures on electrical components. The results of this study will contribute to the creation of the STS detector for the CBM experiment.

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Acronyms

ADC An analog-to-digital converter

AFE Analog Front End

ASIC An application-specific integrated circuit

CBM Compressed Baryonic Matter

CROB Common readout board

CSA Charge Sensing Amplifier

DAC a digital-to-analog converter

EMU GBTx Emulator

ENC Equivalent Noise Charge

FAIR Facility for Antiproton and Ion Research

FEB Front-end Electronic Board

FEE Front-end Electronics

GSI Gesellschaft fur Schwerionenforschung GmbH

LDO Low-dropout voltage regulator

PCB a printed circuit board

QCD Quantum Chromodynamics

STS Silicon Tracking Systems

1 Introduction

Curiosity has driven humans into exploring and understanding the universe around us. Without fully understanding, humans began to come up with models, frameworks, and theories that tried to understand and explain the different phenomena observed in the world around us. Though, mankind had never seen as many breakthrough discoveries as in the past few centuries. Every new achievement opens the paths to another, thus providing an avalanche effect into developing new frameworks, ideas, models, theories, and therefore, technology advancement. We, humans, understood the universe around us so much, that in just a few centuries we came up with the models explaining physics of the very small, down to the sizes of quarks and leptons, all the way to the tremendous scales of the stars, nebulas, galaxies and the universe itself. Fundamental particles and interactions between them can be described by the quantum field theory on a very excellent level of precision, which incorporates quantum mechanics and Einstein's special theory of relativity, while Einstein's theory of General relativity addresses gravity, not as a force, but rather the curvature of the space-time. Attempts on combining these theories to form a unified theory of the universe so far have been unsuccessful. Heavy ion physics studies high-energy atomic nuclei. Heavy ions colliding at relativistic speeds form exotic strongly interacting matter. In the centers of neutron stars, where extreme pressures and densities cause protons and neutrons to combine into exotic states of baryon matter, these states are believed to exist. Compressed Baryonic Matter is an experiment that attempts to investigate this phenomenon. Accelerators are the major instruments for investigating and understanding the architecture of the universe. Modern technology allows us to detect and study subatomic particles produced by collisions at accelerator facilities. Semiconductor devices have been a breakthrough in designing and developing high-precision detector systems for subatomic particles. Silicon strip detectors are a form of semiconductor particle detector used to detect charged particles in heavy ion physics experiments.

1.1 GSI FAIR

FAIR is going to be one of the world's largest and most intricate accelerator facilities. The FAIR accelerator facility will have the unique ability to produce particle beams composed of all chemical elements (or their ions) and antiprotons. In the FAIR accelerator facility, particles will be accelerated to nearly the speed of light, of exceptional intensity and quality, and available for scientific experiments. The FAIR facility includes a superconducting ring accelerator with a circumference of 1,100 meters, storage rings, and experiment sites with a total of several kilometers of the beam line. The GSI existing accelerator infrastructure will serve as the basis for the new FAIR facility[9].

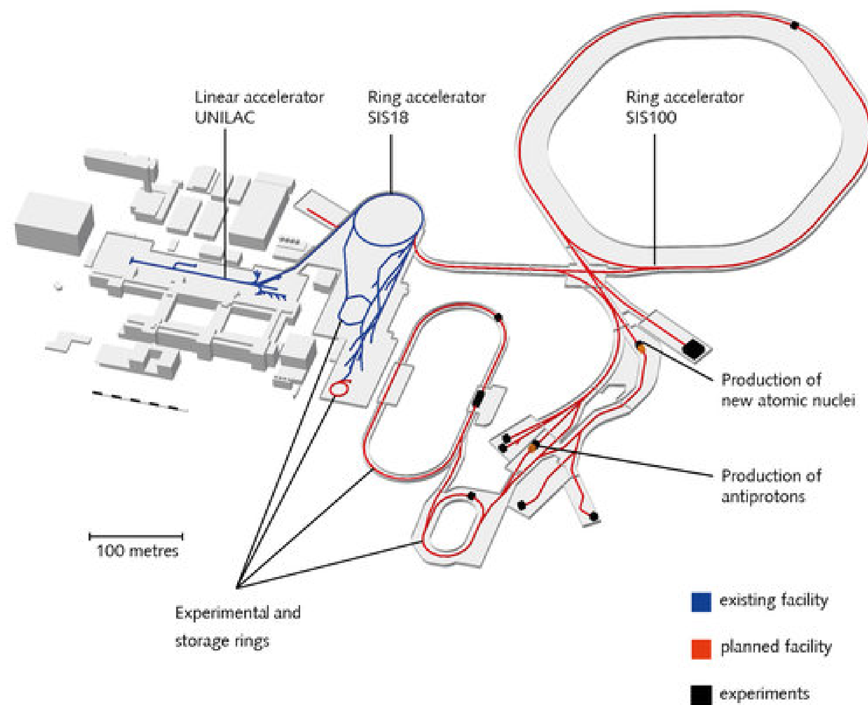

Figure 1: GSI FAIR facility plan. Blue represents already existing facilities, red - facilities under construction [9]

These beams will predominantly support four collaborations: APPA (Atomic, Plasma, and Applications), CBM (Compressed Baryonic Matter), NuSTAR (Nuclear Structure, Astrophysics, and Reactions), and PANDA (anti-Proton ANihilation at DArmstadt).

1.2 CBM experiment

Experiments involving heavy-ion collisions at high energies are devoted to the study of strongly interacting matter under extreme conditions. Intriguing observations have been made at the Relativistic Heavy Ion

Collider (RHIC) at Brookhaven National Laboratory (BNL) that support the theory that partonic degrees of freedom predominate in the early phase of the fireball evolution. The Large Hadron Collider (LHC) at CERN, is used to continue these studies at even greater energies. The purpose of the RHIC and LHC experiments is to investigate the properties of deconned Quantum Chromodynamics (QCD) matter at extremely high temperatures and relatively insignificant net baryon densities. FAIR in Darmstadt and Super-Proton-Synchrotron (SPS) at CERN, address the QCD phase diagram section with the highest net-baryon densities at moderate collision energies,[6, p. 612].

The primary goal of the CBM experiment is to use the SIS-100 accelerator facility at FAIR, Darmstadt with beam energies up to 11 AGeV for Au+Au ion collisions to study the nuclear matter and its degree of freedom in the area of high net baryon density and moderate temperatures [3]. Additionally, the research involves looking into exotic nuclei and the domain where hadronic and partonic matter coexist.

1.3 Detector system for the CBM

One of the planned experiments within FAIR facility is CBM. In order to examine the QCD phase diagram in the region of high net baryon density and moderate temperatures, the CBM, a fixed target heavy-ion experiment, uses variable beam energies from several heavy-ion sources ranging from 2 AGeV to 11 AGeV. The CBM experiment is built to operate at high event rates: $\approx 10^9$ Au + Au particles/sec beam intensity with interaction target 1% (10^7 collisions/sec (10 MHz)) and its fixed target shape span the polar angle between 2.5° to 25° to accept the forward and midrapidity. The technical difficulty of the CBM experiment is to distinguish between hadrons and leptons while filtering out uncommon probes at reaction speeds up to 10 MHz with up to 1000 charged particles per event. Extremely quick and radiation-resistant detector components are needed for measurements at these high rates as opposed to sluggish detectors like Time-Projection Chambers (TPC). The experiment must also include high-resolution secondary vertex determination, lepton identification, a high-speed trigger, and a data collecting system. An extensive acceptance dipole magnet will house the silicon tracking and vertex detector at the upstream part of the detector setup [6].

The key detector of the CBM experiment setup is STS. The STS comprises low-mass silicon micro-strip detectors. With a momentum resolution of about 1 %, the STS enables track reconstruction over a broad momentum spectrum, from about 100 MeV to more than 10 GeV [6].

For the purpose of identifying D^+ mesons, secondary vertices will be precisely determined using the Micro-Vertex Detector (MVD). Two layers of Monolithic Active silicon Pixel Sensors (MAPS), which are placed close to the target, make up the two layers of the MVD. A Ring Imaging Cherenkov (RICH) detector will be used to monitor electrons with momenta under 8–10 GeV/c, and a Transition Radiation Detector (TRD) will be used to measure electrons with momenta over 1.5 GeV/c [6].

A muon tracking chamber and iron layer active hadron absorber device will be used to measure muons

(MuCh). The MuCh will be shifted to the RICH's position for muon measurements. A wall of RPCs will be placed 10 meters behind the target to conduct a time-of-flight (TOF) measurement for the goal of identifying charged hadrons [6].

A Forward Spectator Detector (FSD) is required for identifying the collision centrality and the direction of the reaction plane, and an Electromagnetic Calorimeter (ECAL) that provides information on photons and neutral particles in specific regions of phase space enhances the system [6].

Online event selection, a fundamental component of the CBM experiment, demands free streaming read-out electronics, quick algorithms, and computer farms with future many-core architectures. The CBM detector components required for the measurement of the different observables are depicted in Fig. 2 and detectors with their corresponding particles (the ones that will be tracked by these detectors) are shown in Table 1

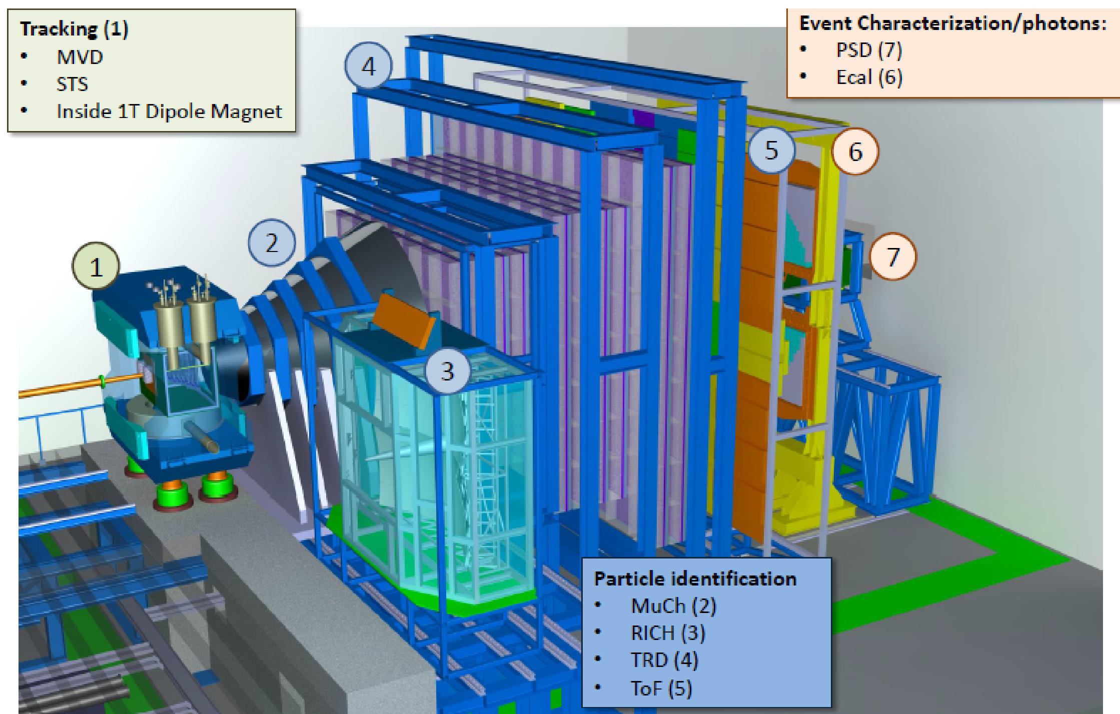

Figure 2: 3D model of a CBM detector setup with individual detectors specified. [6]

Observables	MVD	STS	RICH	MuCh	TRD	RPC	ECAL	PSD
π, K, p		X	(X)		(X)	X		X
Hyperons		X			(X)	(X)		X
Open charm	X	X	(X)		(X)	(X)		X
Electrons	X	X	X		X	X		X
Muons		X		X		(X)		X
Photons							X	X
Photons via e± conversion	X	X	X		X	X		X

Table 1: Observables and corresponding detectors. Background can be suppressed using the detectors marked with an (x) [6].

1.4 The Silicon Tracking System

The STS, which is housed inside the dipole magnet, serves as the primary detector for the CBM experiment and offers track reconstruction and momentum determination of charged particles from beam-target interactions. The detection system must function both during the CBM physics program's startup phase at SIS-100 with ion beam energies ranging from 2 to 14 AGeV and protons up to 29 GeV, and subsequently at SIS-300 with ion beam energies as high as 45 AGeV and protons as high as 90 GeV. It will have thermally insulating walls around it so that the silicon sensors can operate in a cold, dry environment in the radiation field. Of all CBM detectors, it has the highest bandwidth and granularity requirements. It also presents difficulties that are distinct from those presented by other silicon strip detectors frequently utilized in massive high energy physics investigations.[6].

1.4.1 Objectives and design requirements

The CBM experiment's primary tracking detector is STS. The detector must provide high-precision (95% for $p > 1$ GeV/c track reconstruction for charged particles. The STS is made up of 896 double-sided silicon micro-strip sensors, which are placed in 8 tracking stations and cover a $2.5° \leq \theta \leq 25°$ physics aperture. The usual track multiplicity can reach up to 700 percenter Au+Au collision. The STS must be able to measure Au+Au interactions at rates up to 10 MHz in order to discover rare probes. The apparatus, as seen in Fig. 3, is positioned inside a 1 T superconducting dipole magnet field, in a volume measuring 2 m^3 between 30 cm and 100 cm downstream of the target [6].

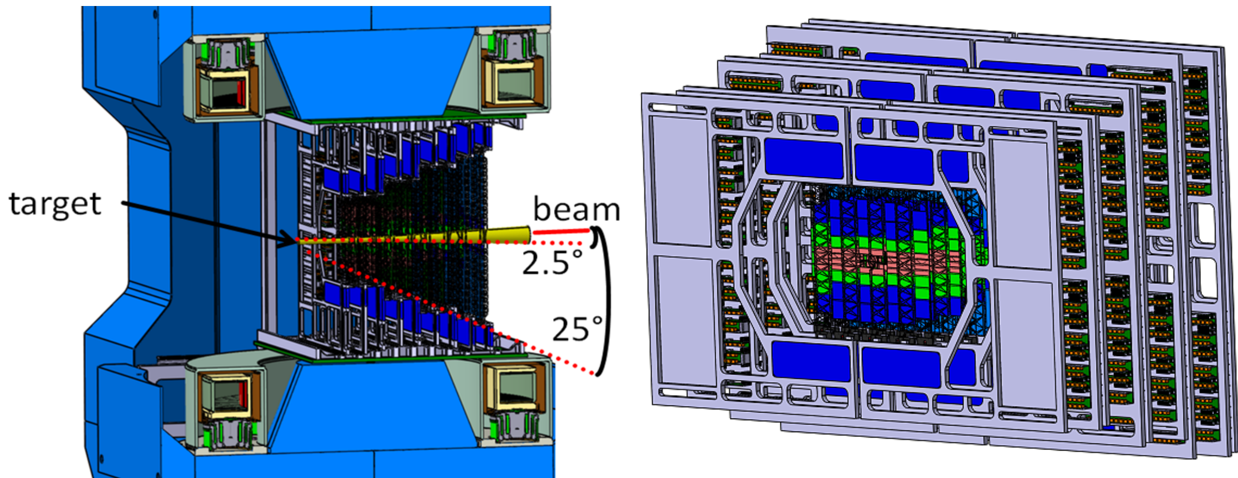

Figure 3: (a) The STS inside the dipole magnet, and the effective area of the detector (b) The STS's eight tracking stations [6]

The following is a summary of some of the most crucial design constraints taken into account when designing the system [12]:

- The configuration needs to be housed within the superconducting CBM dipole magnet, which has a volume of roughly 1.4x2.3x1.3 m^3;
- Multiple scattering dominates the momentum resolution, hence the STS material budget must be as little as feasible, to achieve this low-mass carbon ladders have been designed
- Single hit resolution suggested by the simulations equals 25μ m. A read-out strip pitch 58μm was chosen to achieve the desired resolution.
- Without a hardware trigger, the detector must be able to measure up to 700 particles per center Au+Au collision at interaction rates up to 10 MHz and to avoid pile-up events signal to shape time fast self-triggering Front-end Electronic Board (FEB) have been designed to achieve 20 ns shaping time. Boards must maintain consistent performance in a radiation environment of up to 100 krad/yr
- The system requires radiation-hard silicon sensors, capable to withstand up to 10^{13} 1 MeV n_{eq} during the operation at SIS100
- to distribute the load on sensors and electronics evenly different size silicon double-strip sensors have been designed
- Sensors will be operated on the reverse bias voltages up to 500 V at a temperature around $-5°$ C to reduce radiation damage and leakage currents introduced by it
- Ultralight readout wires up to 50 cm long are used to transmit a sensor signal to the FEE. Such a wire arrangement is comparable to 213 μmeters of silicon for a single detector module
- A powerful cooling system that can remove up to 50 kW of heat from the detector box's inside must be installed.

1.5 Motivation

1.5.1 Heat production

A thermally insulated box containing the STS detector is fitted inside of the dipole magnet aperture. The STS and MVD detectors, as well as the target and the beam pipe, are all supported by this box. A constant 50 kW of thermal power will be produced by the entire system while it is in operation. The major contribution comes from the FEB (about 40 kW), while the remaining energy is mostly produced by low-voltage power connections, heat transfer via the STS box's walls, and a tiny amount from the sensors themselves (around 6 mW/cm^2). The increase in the operating temperature leads to an increment in the detector leakage current.

This has implications for the shot noise, which is proportional to $\sqrt{I_{leak}}$. In addition, the detector leakage current increases with the irradiation dose. Thereby, the excess of heat can cause the thermal runaway of the whole detector [16].

1.5.2 Cooling

The cooling system's responsibility is to guarantee that sensors work at a temperature of no more than -5°C. Gas convection is used in the STS volume because the heat transport inside the physical acceptance should be accomplished with the least amount of material possible. Low humidity is also necessary to prevent condensation on the sensors. Because CO_2 has a high volumetric heat transfer coefficient, evaporative heat transfer based on CO_2 is preferred for cooling electronics. At the top and bottom sides of the STS, the cooling blocks will be securely linked to the boxes containing the Front-end Electronics (FEE).

In the nominal operation scenario, the FEBs are powered on and cooling liquid (NOVEC) is flowing at $-40°C$ through the cooling plate. In this case, simulations indicate that the cooling plate will reach temperatures of -28 to -35°C [2], as shown in the Fig. 4

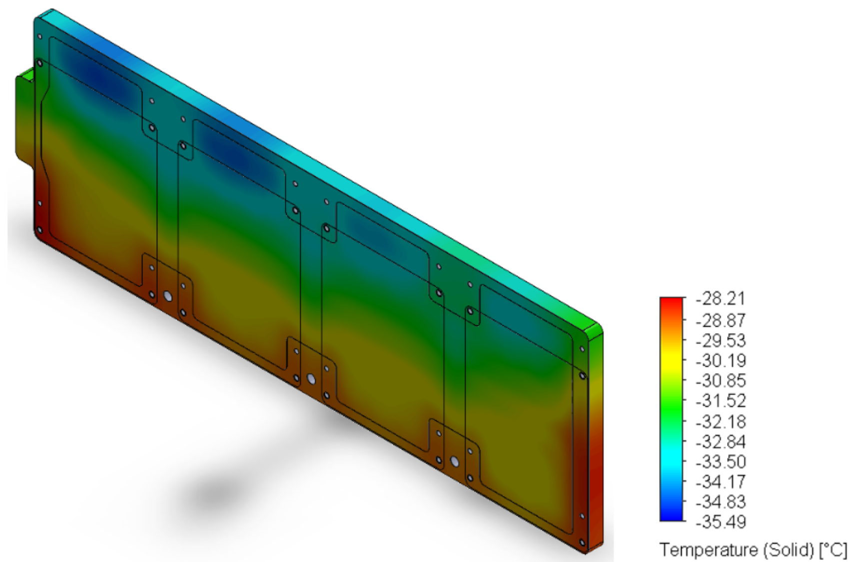

Figure 4: The thermal simulation of the cooling fin [2]

1.5.3 Characterization of CBM STS detector modules

The STS modules are the major building blocks of the STS detector. As already discussed earlier, modules will experience great heat production, high electrical loads, and a radiation environment. The corresponding cooling will be provided, on the one hand, to lessen temperature-related malfunctions, and on the other hand reduce radiation and temperature-related noise, and leakage currents - physical processes that will negatively

affect the measurements made by the STS. Thus, testing the STS modules under such environments is a crucial task for understanding module characteristics and ensuring the STS functionality. Under the scope of this Master's work low temperature-related effects will be investigated.

The STS module is a very complex system, consisting of an electronic board, micro cables, and the sensor. Individually, constituent component physics (such as conductor wires, semiconductor sensors, and micro components) is very well known and understood. Forming a very complex system, an analytical approach for characterizing the STS module is ineffective, requiring experimental investigation of the above-mentioned processes. The following thesis covers two major experiments: **Low-temperature power cycling** of FEBs and **The STS module temperature-dependent noise tests**. The first is required to be investigated and studied separately before addressing the latter, the module tests, to narrow down the intricacy of the module system.

1.5.4 Low-temperature power cycling

Throughout the lifetime of the detector, FEE of the STS will experience significant thermally induced mechanical stresses. During commissioning and configuration, the FEEs, particularly the FEB, will experience a number of power cycles. As reported in CBM progress report [13], the power cycling of the FEBs at a room temperature (approximately 20°C) revealed no problems with the FEB. However, the testing did not replicate STS operational conditions.

Thermal cycling testing is typically conducted to determine the ability of various components and solder joints to withstand extreme temperature fluctuations. If a circuit board is subjected to thermal stresses for extended periods, it may malfunction. Permanent defects to the detector modules' electrical or physical characteristics may compromise their performance. The thermal simulation of the electronic boards is shown in Fig. 5.

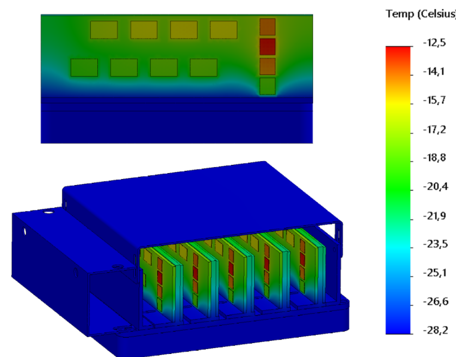

Figure 5: The thermal simulation of the housing of FEBs, greater rectangles represent ASIC microchips while smaller rectangles indicate Low-dropout voltage regulator (LDO)s. The simulation suggests an uneven distribution of the heat over the FEEs [2]

There are several possible power shutdown scenarios that electronics might undergo. First, under the nominal operation operator manually turns the electronics off/on. The radiation-induced soft errors are another possible reason for electronics' sudden power off, and thermal expansion and its effects are therefore hard to predict since it is highly dependent on the errors induced and the time it took for the electronics to be recovered. Another possible scenario is loss of power, which is less probable but still possible. The above possibilities of sudden power cut-off require the STS modules and electronics to be tested and power cycled under operational - low temperatures, to study their limits under such an environment, and investigate possible failure reasons and performance characteristics.

1.5.5 The STS module temperature-dependent noise tests

Understanding STS module characteristics on low temperature and dependence of physical properties on low temperature is a crucial task. Current-voltage characteristics, as well as, noise profile for the sensors are dependent on temperature. Previously made optical inspections on sensors [14] concluded the presence of different grades of defects on the sensors, resulting in each module having slightly different temperature-dependent characteristics. The noise dependencies of the custom-developed microchip-STS XYTERv2 (SMXv2 ASIC) have been previously investigated and the temperature remains one of the main contributors to the chip noise as for the overall noise [12]. Understanding STS module noise characteristics have been conducted analytically and on different scenarios, but due to the complexity of the system, it is impossible to analytically estimate noise characteristics dependence on the temperature thus, motivating the current work on understanding the temperature dependence studies of the STS module noise.

2 Theory

2.1 P-N junction

P-type and N-type doped semiconductor is used to make silicon detectors. Elements with the valence number three (such as boron) and five (such as phosphorus) are used to dope each type, in turn, to create silicon's P-type and N-type, respectively. As a result, the P-type has a large concentration of charge carriers holes whereas the N-type has a high concentration of electrons.

A P-N junction is created when P-type and N-type semiconductors are placed near one another, as seen in Fig. 6.

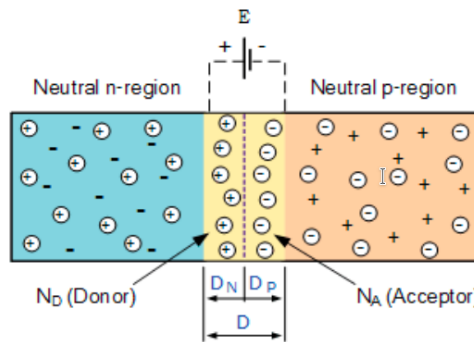

Figure 6: p-n junction in the semiconductor device [10].

Diffusion happens close to the junction as a result of the varying concentration. Diffusion leads to charge accumulation in an area close to the p-n junction interface. As opposed to the n-type, which has holes close to the junction, the p-type has an area near the contact that acquires electrons. A Space Charge Region (SCR), also known as a depletion zone, is created when electrons and holes aggregate close to the p-n junction region. Drift currents flow in the opposite direction of diffusion currents due to an electric field created across the junction by space charge. When the opposing electric field stops allowing the charge to traverse the junction, an equilibrium is reached. The potential across the junction is usually referred to as a built-in voltage. The value of the built-in voltage for the silicon detector is $\approx$ 0.6 eV. Built-in potential on a junction can be described as [17]:

$$V_{bi} = \frac{kT}{q} ln(\frac{p_{p0}}{p_{n0}}) = \frac{kT}{q} ln(\frac{n_{n0}}{n_{p0}}) \tag{1}$$

where:

n = Electron density
p = Hole density
$n0$ = Electron side
$p0$ = Hole side

Space charge distribution pattern holds essential information for understanding the physical properties across the p-n junction. The distributed charge generates an electric field. Integrating an electric field across the junction provides the potential difference., see Fig. 7 [17].

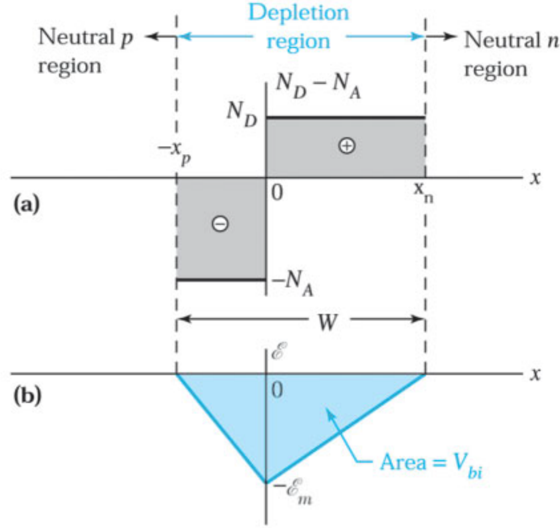

Figure 7: (a) Space charge distribution in the depletion region at thermal equilibrium. (b) Electric-field distribution.[17]

The depletion layer width can be related to the built-in voltage according to the equation [17]:

$$W = \sqrt{\frac{2\epsilon_S}{q}(\frac{N_A + N_D}{N_A N_D})(V_{bi} - \frac{2kT}{q})} \tag{2}$$

where:

N_A = Acceptor concentration
N_D = Donor concentration
ϵ_S = Permittivity
q = elementary charge
k = Boltzmann constant
T = Absolute temperature

The depletion layer capacitance is defined by [17]:

$$C = \frac{dQ_c}{dV} \tag{3}$$

There are two limiting diffusion profiles: Abrupt junction - alloying and shallow diffusion and Linearly graded junction - deep diffusion. An abrupt junction is just a model, in reality, it is impossible to create an abrupt junction and numerical analysis is necessary to investigate the doping profile. Like abrupt junction, similar behavior can be plotted for the linearly graded junction depicted in Fig. 8 [17].

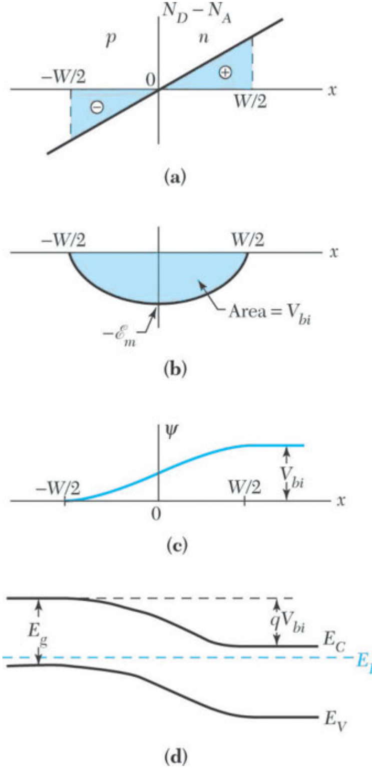

Figure 8: Linearly graded junction in thermal equilibrium. (a) Impurity distribution. (b) Electric field distribution. (c) Potential distribution. (d) Energy band diagram. [17]

For linearly graded junction the linear capacitance can be obtained:

$$C_j = \frac{\epsilon_s}{W}\left(\frac{qa\epsilon_s^2}{12(V_{bi}-V)}\right)^{1/3} \tag{4}$$

where:

a = impurity gradient (cm^{-4})

2.2 Current-voltage characteristics

If applied external voltage, the Fermi level shifts on the energy band diagram, unlike the p-n junction without any external voltage, where the Fermi level remains the same across the p-n junction. This phenomenon

gives a rise to so-called Quasi Fermi levels. The energy band diagram, Fermi level, and carrier distributions for reversed and forward bias are shown in the Fig. 9 [17]

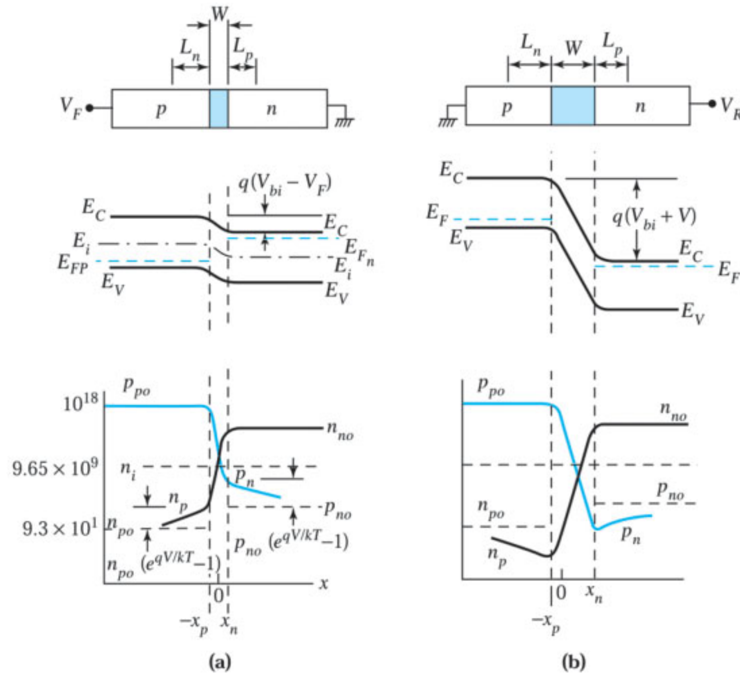

Figure 9: Depletion region, energy band diagram, and carrier distribution. (a) Forward bias. (b) Reverse bias. [17]

Current density across the p-n junction can be characterized in relation to voltage. This equation is called the Shockley diode equation [16, p. 456]. Graphically this dependence is depicted in Fig. [17].

$$J = J_s(e^{\frac{qV}{kT}} - 1) \tag{5}$$

where:

J_s = saturation current

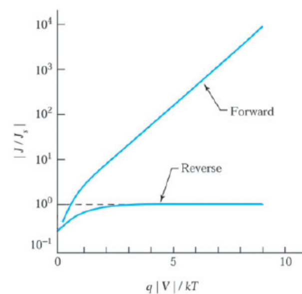

Figure 10: Ideal current-voltage characteristics [17].

2.3 Generation and recombination in p-n junction

Impurities, in the semiconductors, can introduce intermediate energy levels between the conductance and valence bands, these bands are called traps. Traps can mediate the transition of electrons and holes in between conductance and valence bands. In the reverse bias regime, one can discuss the electron-hole pair generation rate assuming $pn \ll {n_i}^2$ using the Shockley-Read-Hall recombination equation and assumption: $n, pn_i \to (np - n_i)^2 \approx -{n_i}^2 \to$

$$U = -(\frac{\sigma_p \sigma_n \nu_{th} N_t}{\sigma_n \exp(\frac{E_t - E_i}{kT}) + \sigma_p \exp(\frac{E_i - E_t}{kT})}) n_i = -\frac{n_i}{\tau_e} = -G \tag{6}$$

where:

τ_e = Effective lifetime
G = Generation rate
$\sigma_{p/n}$ = capture cross sections for holes/electrons
ν_{th} = thermal velocity
E_t = Trap energy
E_i = Intrinsic Fermi energy
N_t = Trap concentration

Now, we one can obtain generation current j_{gen} over integrating the depletion width:

$$j_{gen} = \int_0^W q|U|dx = \int_0^W qGdx = q|U|W = \frac{qn_iW}{\tau_e} \tag{7}$$

generation current depends on the depletion width. Bias-dependence of W for an abrupt p-n junction $\to j_{gen} \approx (V_{bi} + V)^{1/2}$. Total reverse current (for $p_{n0} \gg n_{p0}$ and $|V|\, 3\frac{kT}{q}$) = diffusion current + generation current in the depletion region assuming $(N_A \gg N_D)$

$$j_R = q\sqrt{\frac{D_p}{\tau_p}\frac{n_i^2}{N_D}} + \frac{qn_iW}{\tau_i} \tag{8}$$

Where:

D_p = Diffusion constant (Einstein's relations)

2.4 Working principle of silicon semiconductor detectors

A semiconductor detector built of silicon functions similarly to a gaseous detector. The charged particle that passes through the detector ionizes, producing a primary electron-ion pair. The generated ions and electrons are gathered at the electrodes. When using a silicon detector, a reverse bias voltage is used. A sensor must be completely depleted in order to be used as an active volume for the formation of electron-hole pairs and to measure the maximum amount of energy that a charged particle may deposit. An increase in the reverse

bias voltage can be used to accomplish this. The equation 2 for the depletion width of p-n junction can be simplified and rewritten [16, p. 65]:

$$W_d = \sqrt{\frac{2\epsilon(V_b + V_{bi})}{eN_d}} \tag{9}$$

Where:

N_d = a dopant concentration, ϵ is a dielectric constant

Along the particle track, an electron, and a hole is created as the charged particle passes through the sensor. Under the influence of the electric field, the newly created electrons and holes begin traveling in the opposite direction. The charge creation and acquisition process is described in Fig. 11.

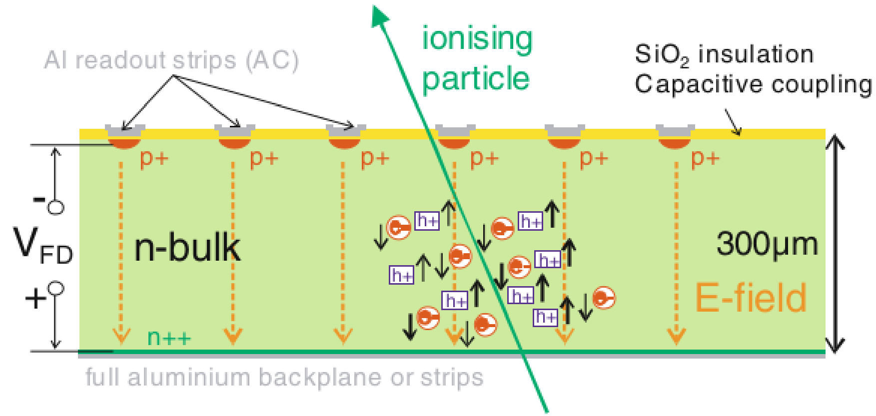

Figure 11: Ionising particle passing through the sensor in the reverse bias regime [7]

According to Ramo's theorem, the charges in the silicon bulk that are drifting cause signals to be produced on the appropriate electrodes [16, p. 75].

$$i_c = e \cdot \vec{E_w} \cdot \vec{v_c} \tag{10}$$

Where:

c = type of charge carriers
$\vec{E_w}$ = weighting field

By grounding the other nearby electrodes and providing a unit voltage to one electrode, the weighted field is created. By doing an integration over time, the charges released by the silicon material are provided:

$$Q = \int_{t_0}^{t} i_t dt \tag{11}$$

Sensors operated under the forward or reverse bias regime exhibit different current to voltage dependence. Shockley equation for an ideal diode can be rewritten for currents as

$$I = I_n + I_p = I_0(e^{eV/kT} - 1) \tag{12}$$

Where:

I_O = Saturation current
e = elementary charge
k_β = Boltsmann constant
T = absolute temperature

Sensors operated under the reverse bias regime will have a negative voltage in the exponential term, meaning that when V becomes much more significant than e/kT exponential term becomes negligible and the current saturates. Also, eq. 12 suggests that the current flow is reversed under reverse bias.

2.5 Noise

There are many sources of noise in complex electronics systems. To understand these sources the spectral distribution of the noise needs to be studied. One of the most expected sources of noise is fluctuations in the velocities of the charge carriers. While the current flows, charge carriers are transported with a drift velocity. However, as the temperature rises from zero, these fluctuations in the velocity contribute to noise generation. In p-n junction the probability of the charge carriers overcoming the barrier is not interrelated, In the reverse-biased regime independent generation-recombination influences the current, this type of noise is called shot noise which also holds a white spectrum. Another process is called trapping of the charge carriers when the imperfections, or in other words impurities are introduced in the semiconductor. After some characteristic time, these charge carriers are released thus contributing to a more specific portion of bandwidth. There are a few notions needed to understand noise physics. A spectral distribution of power density dP_n/df, voltage and current distributions - $dv_n/df \equiv e_n$; $di_n/df \equiv i_n$ [16].

2.5.1 Thermal (Johnson) noise

Due to fluctuations thermal noise arises. The noise in the resistors with the resistance of R can be described with spectral noise density against the frequency [16]:

$$dP_n/df = 4kT \tag{13}$$

Where:

k = Boltzmann constant
T = Absolute temperature

Power dissipated in the resistance is described as:

$$P = \frac{v^2}{R} = i^2 R \tag{14}$$

Spectral voltage noise density can be derived from eq. 13 and eq. 14

$$\frac{dv_n^2}{df} = e_n^2 = 4kTR \tag{15}$$

Spectral current noise density can be derived from eq. 13 & eq. 14

$$\frac{di_n^2}{df} = i_n^2 = 4kT/R \tag{16}$$

2.5.2 Shot noise

Spectral density for Shot noise can be described as [16]:

$$i_n^2 = 2eI \tag{17}$$

Where

e = Electron charge
I = Average current

2.5.3 Low frequency "1/f noise

Spectral density for "shot noise" can be described as [16]:

$$v_{nf}^2 = \int_{f1}^{f2} \frac{A_f}{f} df = A_f \log \frac{f_2}{f_1} \tag{18}$$

Where: $A = fe_{nf}^2$

2.6 Noise in the STS module

In the STS module layout there are a few significant sources of the noise: Thermal noise due to resistive materials shot noise due to the detector leakage current, and charge-sensitive amplifier intrinsic noise. Amplifiers are prone to express a "white" noise spectrum at high frequencies. Such noise is dependent on Charge Sensing Amplifier (CSA) parameters and transconductance [22]. These estimates have been made to be described as follows [21], [23]:

$$e_{na}^2 \approx 4k_B T \alpha\gamma / g_m \tag{19}$$

Where

α, γ = CSA parameters
g_m = transconductance

At low frequencies the noise dependence is defined by a more predominant parameter, the so-called flicker noise - K_f/f. The K_f coefficient is characteristic of the CSA. For complex systems, such as STS modules, the equivalent diagram can be drawn to address noise sources analytically, see Figure 12 [22] [12].

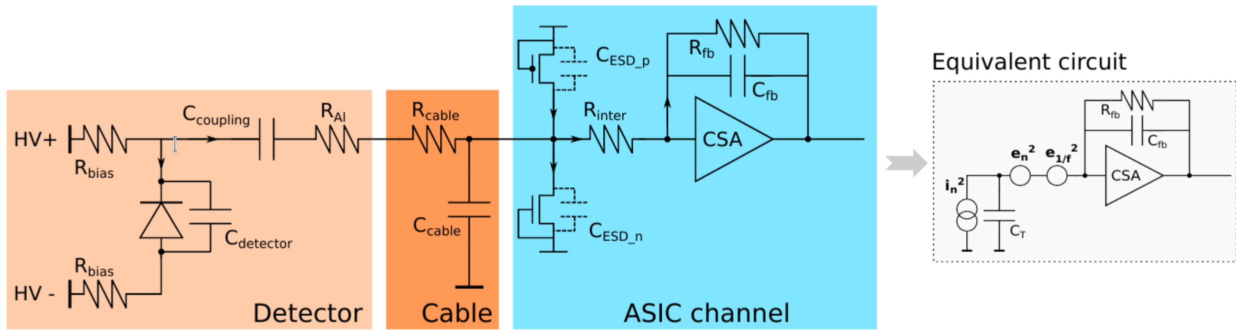

Figure 12: Simplified diagram describing STS module [12]

To analytically estimate the noise for the STS module system, total noise can be broken down into three different equivalent noise sources [12]:

1. Parallel current noise (i_n^2)

$$i_n^2 = \frac{4k_B T}{R_{bias}} + \frac{4k_B T}{R_{fb}} + 2eI_{det} + 2eI_{ESD_n} + 2eI_{ESD_p} \tag{20}$$

2. series voltage noise (e_n^2)

$$e_n^2 = 4k_B T R_{Al} + 4k_B T R_{cable} + 4k_B T R_{inter} + e_{na}^2 \tag{21}$$

3. series $1/f$ noise ($e_n f^2$):

$$e_{nf}^2 = \frac{K_f}{f} \tag{22}$$

The total noise or Equivalent Noise Charge (ENC) can be evaluated with the integral of frequency bandwidth and the amplifier frequency-dependent gain $A(f)$ [12]:

$$ENC^2 = \int_0^\infty (i_n^2 + e_{nf}^2 + e_{nf}^2) A(f) df \tag{23}$$

Evaluating the integral and considering the total capacitance for the module [12]: $C_T = C_{det} + C_{cable} + C_{ESD_n} + C_{PCB}$, Eq. 23 yields:

$$ENC^2 = \underbrace{i_n^2 F_i T_s}_{\text{current noise}} + \underbrace{e_n^2 F_v \frac{C_T^2}{T_s}}_{\text{voltage noise}} + \underbrace{F_{vf} A_f C_T^2}_{\text{1/f noise}} = ENC_i^2 + ENC_e^2 + ENC_{1/f}^2 \tag{24}$$

F_i, F_v, F_{vf} = the weighting coefficients
T_s = $characteristictimefor$CR-(RC)^2 STS shaper

3 Experiment

3.1 STS module components

The detector module is the essential structural component of the STS. It is made up of two front-end boards (FEB) and a double-sided silicon sensor coupled with micro cables. Each sensor side has a double side of 1024 strips and is linked to a FEB that houses 8 specifically created ASICs. A pair of micro cables conveying the analog signals to the FEE is linked to groups of 128 strips.

Modules with different form factors (sensor sizes and micro cable lengths) will be manufactured depending on their location in the detector. The 8 tracking stations will be filled with a total of 896 modules that are installed onto 106 carbon-fiber ladders. A detector module prototype is shown in Fig. 13.

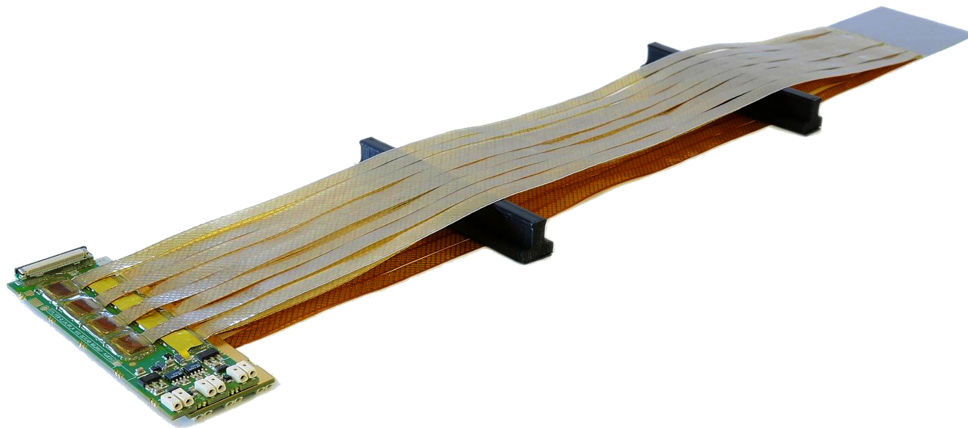

Figure 13: The STS's functional foundation is the detection module. Each module consists of a silicon sensor with two sides that are linked to the FEBs by a double stack of micro cables. [12]

3.1.1 Silicon sensors

Numerous high-energy physics experiments have used silicon microstrip sensors with great success [4] [11]. A technology double-sided silicon microstrip sensor array will be used in the STS. Sensor thickness is 300 μ meters. Sensor width measures 6.2 cm while the length comes in three different measures, 2.2, 4.2, 6.2, and 12.2 cm. The sensor length used for noise tests is 6.2 cm. The strip pitch measures 58 μ meters. While front-end and back-end strips have a stereo angle of 7.5° [1].

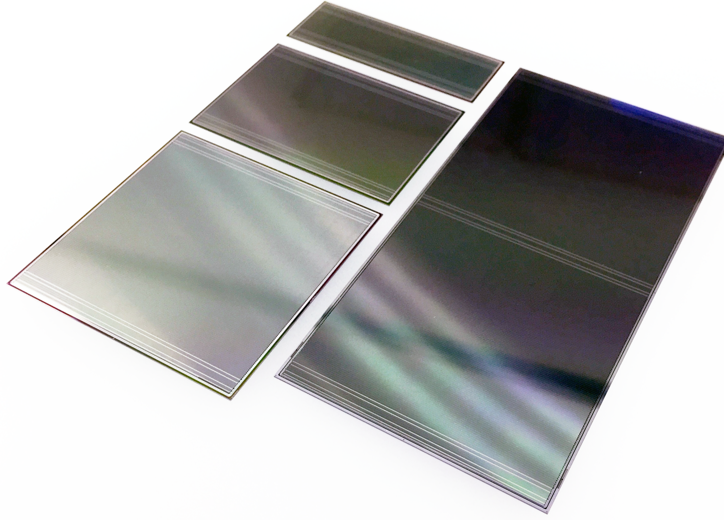

Figure 14: family of silicon CBM06 trackers for the system. Sensors built with the same width of 6.2 cm and four different strip lengths (2.2 cm, 4.2 cm, 6.2 cm, and 12.4 cm). [12] [1]

Pre-experiment evaluation of the sensors has been performed on different versions of prototype sensors. Testing and operating software have been developed. Leakage current and capacitance characteristics have been evaluated in the GSI clean room facility [1].

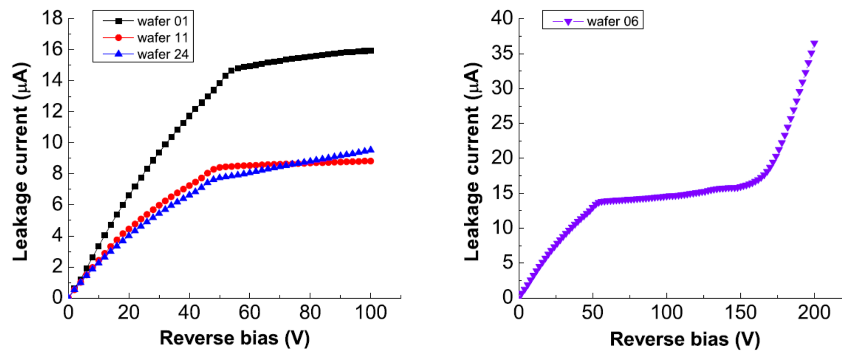

Figure 15: Bulk current on bias voltage dependencies for prototype CBM03 sensor [1]

3.1.2 Front-end Electronics (FEE)

Front-end Electronics or in other words Front-end Electronic Boards (FEB) is the main electronics unit in the STS module. there are two main variations of the FEB: A and B, corresponding to the n and p sides of the sensor accordingly. FEB is a main a printed circuit board (PCB) to house eight XYTER microchips (An application-specific integrated circuit (ASIC)). ASICs are, on the one hand, placed on the FEE and are using its design for powering and communication, on the other hand, they are attached to micro cables that deliver the connection with the sensor. Two pairs of 1.2V and 1.8V low dropout voltage regulators are

installed on one side, aside from voltage input pins, while the other side houses a connector for the data cable. FEBs A and B are mounted on two sides of the cooling fin.

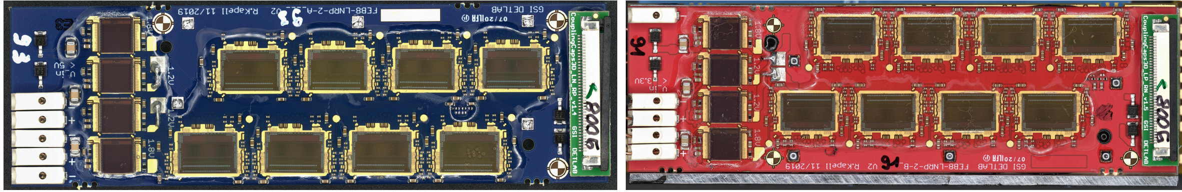

Figure 16: (a) FEB A, (b) FEB B

3.1.3 STS XYTER SMX 2.2

Application-optimized detector readout circuits are essential for new physics experiments at the FAIR in Darmstadt. In the Compressed Baryonic Matter experiment, the STS/MUCH-XYTER family (SMX2.1 and SMX2.2) are 128-channel prototype ASICs for silicon strip detectors and gas electron multiplier (GEM) detectors. They offer self-triggered amplitude and time measurements of incoming charge and serial data transmission. The 10 mm x 6.75 mm microchips were manufactured using the 180 nm UMC CMOS process [18, pp. 1-3], see Fig. 17.

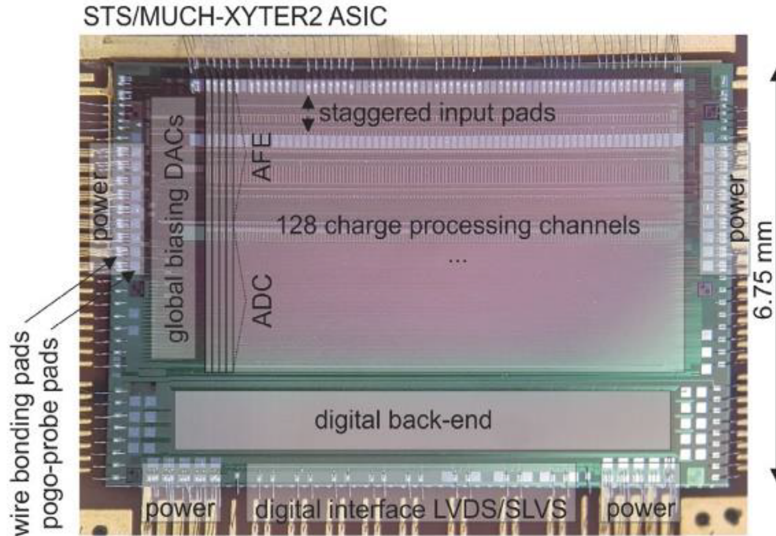

Figure 17: Microscopic photograph of STS SMX 2.2v [18]

Fig. 18 describes the layout of three adjacent channels. The major features of STS XYTER 2.2v are the following [18]:

- 128 Analog Front End (AFE) channels with 14-bit time and 5-bit amplitude measuring circuits.

- Two additional test channels (channels 128, and 129) located on the two sides of the ASIC receive buffered internal signal outputs.
- Registers for full-custom configuration, common biasing blocks, calibration circuits, as well as the band-gap reference voltage and a current source.
- Digital back-end, clocked at 160 MHz, offering access to configuration registers, free-streaming digital readout, timestamp-wise classification of acquired hits and successive serialization with 320 Mbps/link or a maximum of 47 Mhits/s, as well as multiple diagnostic features.

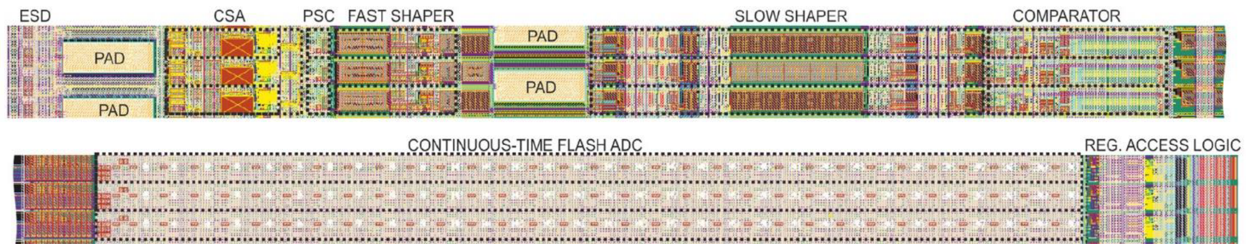

Figure 18: The configuration of three adjacent channels. The channel pitch is 58 μm [18].

Fig. 19 is a schematical representation of one channel depicted in Fig. 18.

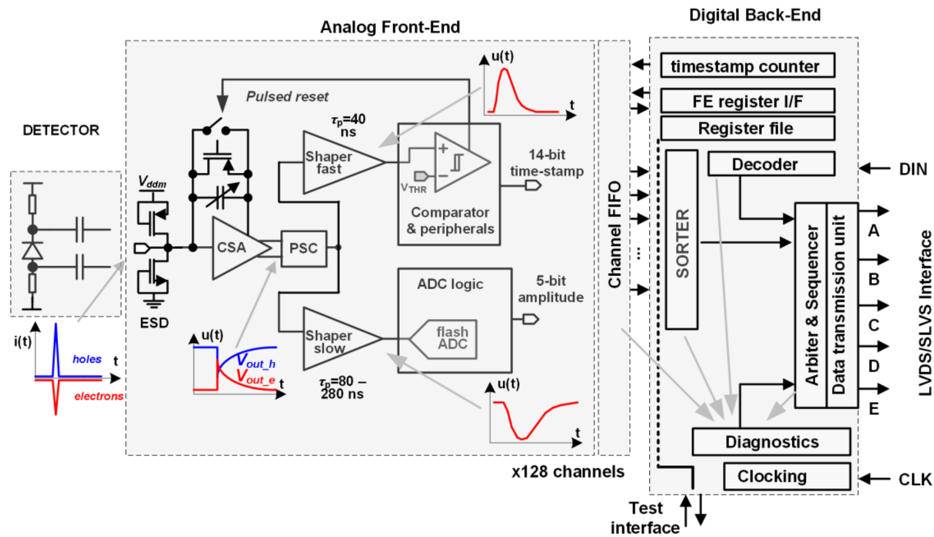

Figure 19: Schematics of a single module channel [8]

3.2 Low-temperature power cycling

3.2.1 Setup

To provide the experimental environment according to requirements, several devices are introduced in the experimental setup. Binder is a "freezer" device that can be operated both manually and remotely. It offers the necessary volume for the STS modules to be housed and is equipped with humidity and temperature sensors. The inner chamber of the binder is pneumatically isolated and humidity and temperature can be very precisely controlled. The binder is depicted in Fig. 20 (a).

Figure 20: (a) Binder, (b) Lauda, (c) Power Supply [15]

Power to electronics is supplied via Hameg - Rhode & Schwarz power supplies, Fig. 20 (c). Connectivity to the server and DAQ is provided by data cables connecting FEB-s to the FPBGA based GBTx Emulator (EMU) readout board [19].

To avoid humidity condensation on electronics, causing an unwanted failure the external chiller-Lauda (Fig.

20 (b)) is delivering 2°C warmer (than the Binder chamber temperature) liquid "Kryo 51" through pipes to the cooling plate, Fig. 21 housing electronics. This method ensures that excessive condensation always happens on the walls of the chamber and never on the electronics, also this setup ensures reliable thermal coupling.

In this setup two sets of FEBs (a total of four units) are mounted using two aluminum-coated fins Fig. 21 (b). FEBs were glued using a thermally conductive adhesive, on fins using predetermined patterns and precise material measurements to ensure thermal coupling and even distribution of the glue.

Each FEB houses two 1.2V digital and two 1.8V analog LDOs, and eight XYTER microchips. Each FEB is supplied with the required power on two channels (four pins) according to the LDO types. There are two kinds of FEBs used type A and type B, they are slightly different in their designs, operating the n and p sides of the sensors accordingly, see Fig. 21 (b).

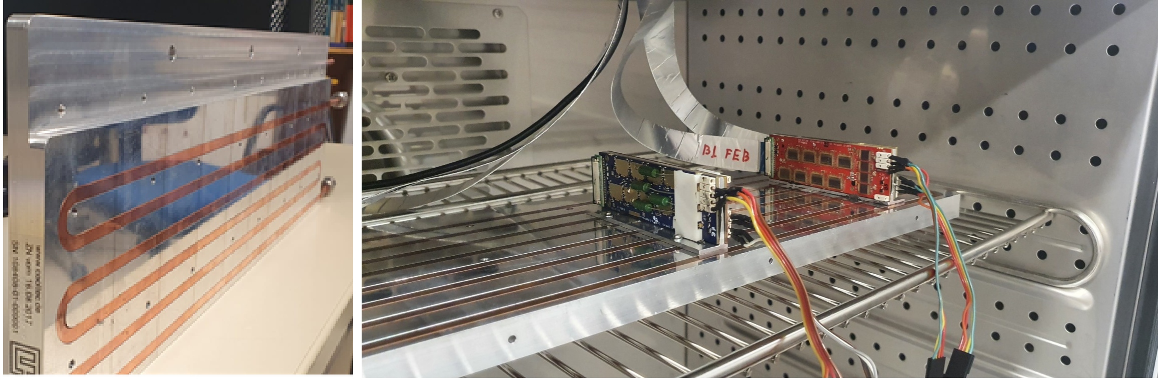

Figure 21: (a) Cooling plate, (b) two sets of FEBs mounted

For monitoring, accessing the database (Redis DB), and recording process variables, the software framework integrates the Control System Studio (Phoebus). With the archiver appliance, all values are stored. Readouts for relative humidity are obtained from the climatic chamber's built-in relative humidity (RH) sensor.

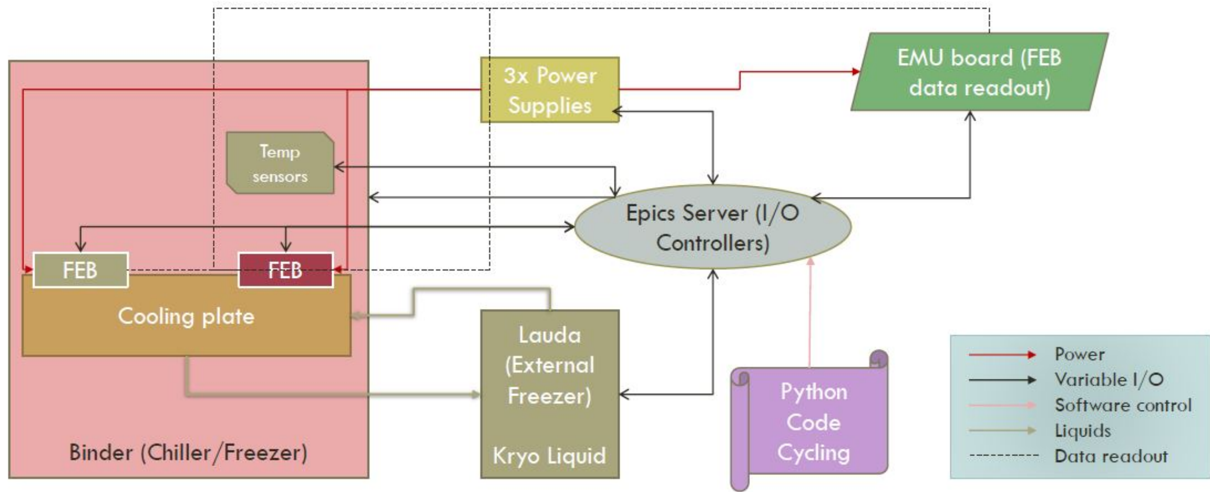

Figure 22: Conceptual design of the Low-temperature power cycling experiment setup

The thermal cycling of the FEBs was the primary goal. The STS-diagnostic XYTER circuit was utilized to find any PCB-related flaws and assess FEB's performance. A specialized soft Input/Output Controller (IOC)2 was used to read the temperatures, VDDM, and CSA bias values. The pyEPICS library was utilized to obtain the abovementioned values, and the GBTxEMU-based readout chain was modified to publish the values through channel access protocol. Simplified conceptual design is depicted in Fig. 22.

3.2.2 Procedure

The experiment procedure covers a similar scenario to what FEBs might experience under the sudden power cut-off at low temperatures. DAQ for power supply and other non-FEB related values is performed consistently. FEB-related DAQ is only performed when the FEB-s are on. Fig. 23 depicts the beginning of the experiment followed by three cycles. The experiment procedure can be described in several steps:

- Binder, Lauda and FEBs are at 20°C
- FEB tests - configuration of XYTER microchips registers and other parameters are being made, charge sensing amplifier voltage values, temperatures and voltages of the microchips - Vddm-s are monitored
- Temperatures are set to −30°C, gradually Binder, Lauda, and electronics temperatures drop.
- FEB tests are conducted
- After reaching −30°C electronics are powered off.
- After a few minutes "lower equilibrium" temperature −30°C is reached

- FEBs are powered back on and tests conducted, three testing cycles on each FEB. Tests heat up FEBs and after approx. 20 minutes upper equilibrium temperature is reached
- Power is restricted again to electronics and the cycle repeats.

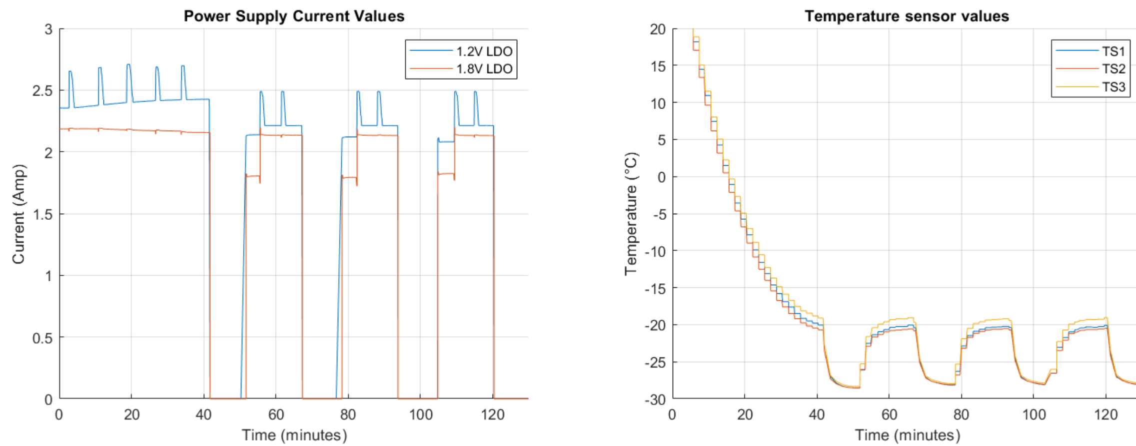

Figure 23: In these figures a graphical representation of the initial stage of the experiment and consecutive three cycles are depicted (a) FEB LDO's current consumption, (b) Temperature Sensor readouts from different positions on the FEB

3.2.3 Results

Overview

In the scope of low-temperature cycling, eleven FEB-s were examined. Eight of them underwent preliminary passive cycling (temperature cycling without FEBs being powered) and active cycling tests (temperature cycling with FEBs powered). FEBs had minor variations, including three distinct combinations of glob top - a covering glue for electrical components, a pair without glob top on the LDOs, and microchips in place of the matching resistors. A and B are the two distinct forms of FEB (corresponding to the n and p sides of the silicon sensor). The table 2 displays the type of FEB variations, as well as the number of cycles performed.

FEB type	Glob-top	Preliminary cycles	Cycles Performed
91B	DYMAX Dam 9008 fill 9001	Passive: 150 Active: 100	150
93A	DYMAX Dam 9008 fill 9001	Passive: 150 Active: 100	150
94A	DYMAX Dam 9008 fill 9001	Passive: 150 Active: 100	150
94B	DYMAX Dam 9008 fill 9001	Passive: 150 Active: 100	150
95A	DYMAX 9001	Passive: 150 Active: 100	250
95B	DYMAX 9001	Passive: 150 Active: 100	250
96B	No ASIC No glob-top on LDO's	Passive: 150 Active: 100	250
97A	No ASIC No glob-top on LDO's	Passive: 150 Active: 100	250
135B	DYMAX 9014	0	100
136B	DYMAX 9014	0	200
138A	DYMAX 9014	0	200

Table 2: List of all the FEBs, that underwent the examination and their descriptions

Analysis, observations, and discussion of for several FEBs of interest will be covered in the next chapters.

Analysis and discussion

Throughout the experiment, multiple variables were measured: the following is a list of the most noteworthy variables: Binder temperature and humidity; Lauda temperature; Power supply voltage and currents; For each FEB and XYTER ASIC microchip voltage (Vddm), CSA voltage, and temperature values. Experiments have lasted several weeks to months; therefore, only the most noteworthy findings will be highlighted. The experiment was preceded and followed with microscopical-optical and electrical inspections every FEB.

FEB 91B: Approximately after 55 hours in the experiment, FEB91 expressed an unusual drop in the LDO current consumption see Fig. 24 (a).

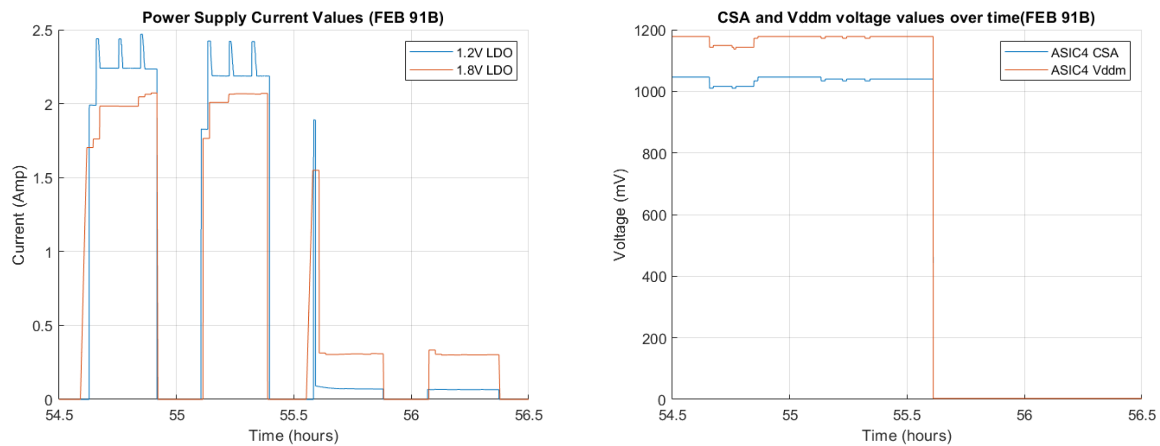

Figure 24: (a) Current consumption of analog and digital LDOs, (b) ASIC voltage - Vddm and CSA voltage

CSA and Vddm voltage drops have been observed for all ASICs. Fig. 24 (b) shows Vddm and CSA values for ASIC 4, the same variable values for all other ASICs expressing similar behavior.

Post-experimental electrical tests conducted by the electrical engineering department confirmed the permanent failure of the FEB 91B. The defect was related to the LDO bonding breaking. Soldering joint disconnection can be related to different thermal expansion coefficients for various materials contributing to LDO joints.

FEB 93A: Reduction of the current consumption of LDOs was observed soon after the environment reached $-30°$C like FEB 91B case. Though, consumption recovered after warming up to 20°C. After observations, in order to exclude connection-related problems, the experiment was restarted but malfunctions maintained to consist soon after reaching low temperatures, see Fig. 25. Fig. 25 (c) depicts the Vddm voltage reading of ASIC2, suggesting that a potential difference was present at the microchip, though with a significant decrease (50 ± 10 mV).

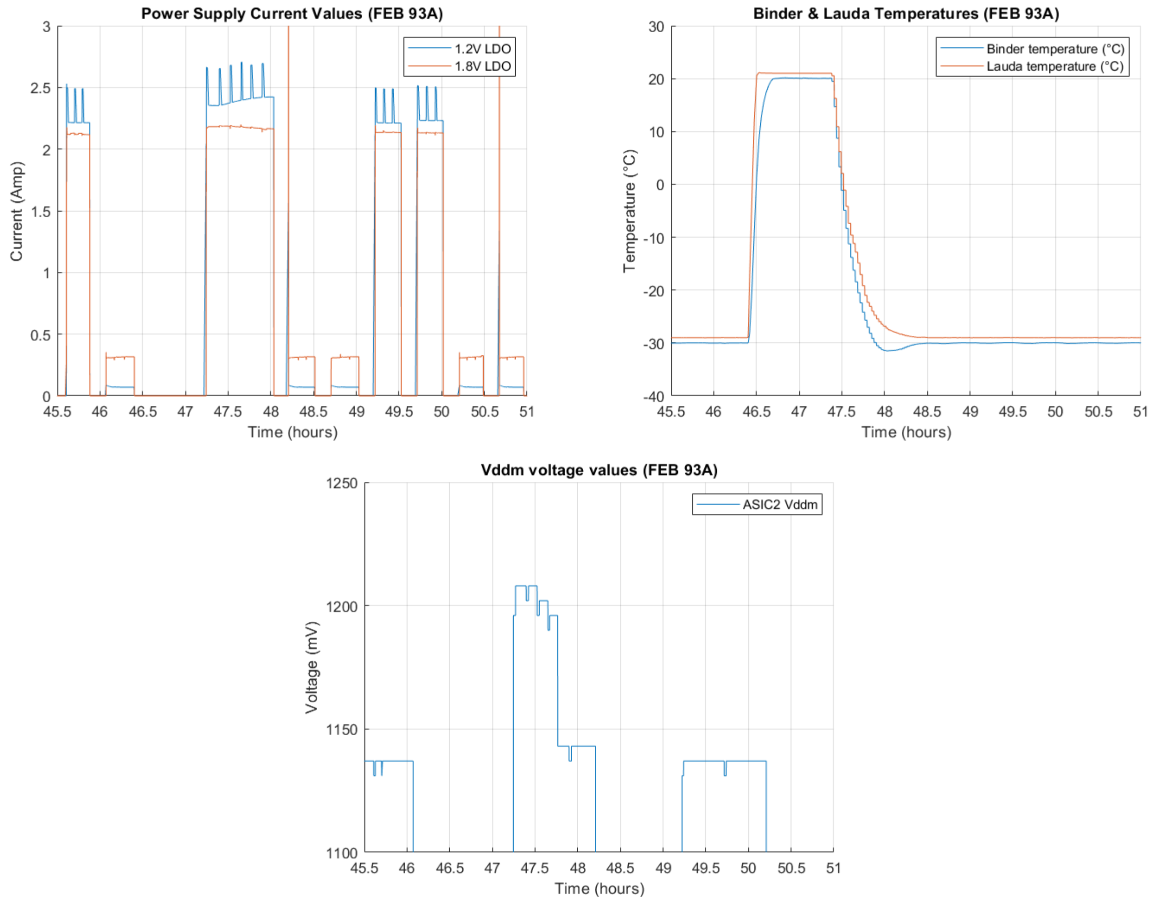

Figure 25: (a) Current consumption of analog and digital LDOs over time, (b) Binder and Lauda temperature measurements, (c) Vddm voltage value for ASIC2

As unusual behavior persisted, preset voltage settings on both LDO inputs were increased by 0.2 volts. At this voltage setting current consumption at peaks was increased by approx. 0.2 A for 1.2 analog LDO. Suggesting that in this environment and power supply cable settings (cable length exceeds 1.5 m), there was a significant voltage drop and 1.2 LDO was operating at the operational threshold, see Fig. 26. Note, that current peak values in Fig. 25 (a) at timestamp 47h-48h exceed 2.5 A, but this is due to the temperature exceeding $-30°$ C as for the initial stage of the experiment. Corresponding Binder and Lauda temperature for Fig. 26 is already at experiment minimum. One ASIC permanently failed to respond to tests.

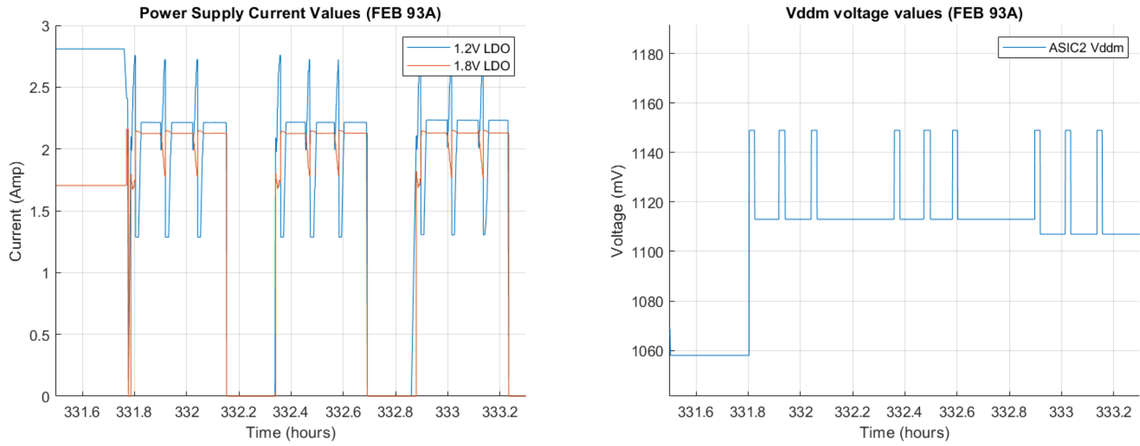

Figure 26: (a) Current consumption of analog and digital LDOs over time, (b) Vddm voltage value for ASIC2

FEB 94A: For FEB94A in the initial stage of the tests all ASICs and their variable readings followed the expected pattern. Approx. after 100 cycles in the experiment (at 332.8 hours on the time axis), power supply current consumption dropped significantly, approx. 5% for 1.8V LDOs and approx. 50% for 1.2V LDOs. The current consumption comparison is depicted in Fig. 28

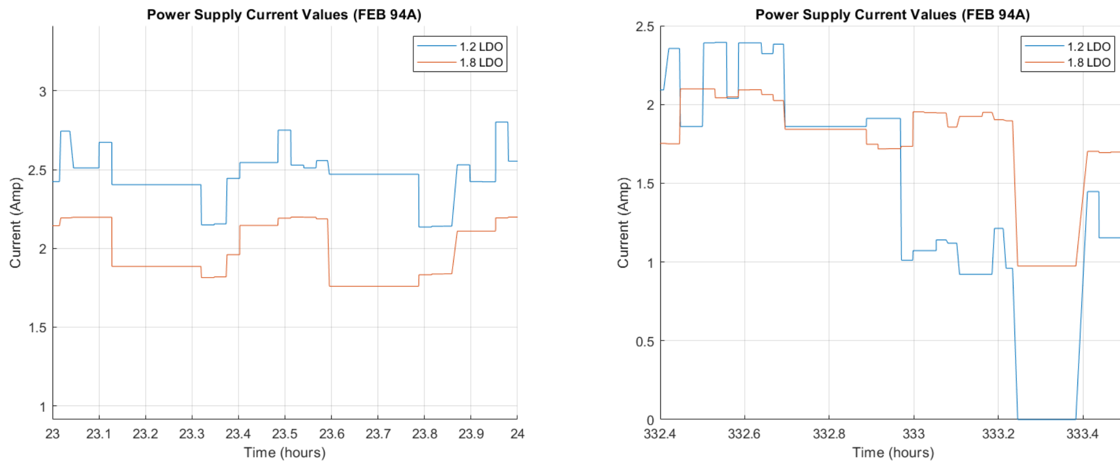

Figure 27: (a) Power supply current values for well-functioning FEB, (b) Power supply current values for malfunctioning FEB

The Vddm and CSA readings on each ASIC dropped to zero for four ASICs when 1.2V LDO current reduction was observed above. Two ASICs followed a normal testing pattern, while the other two did not respond to the tests.

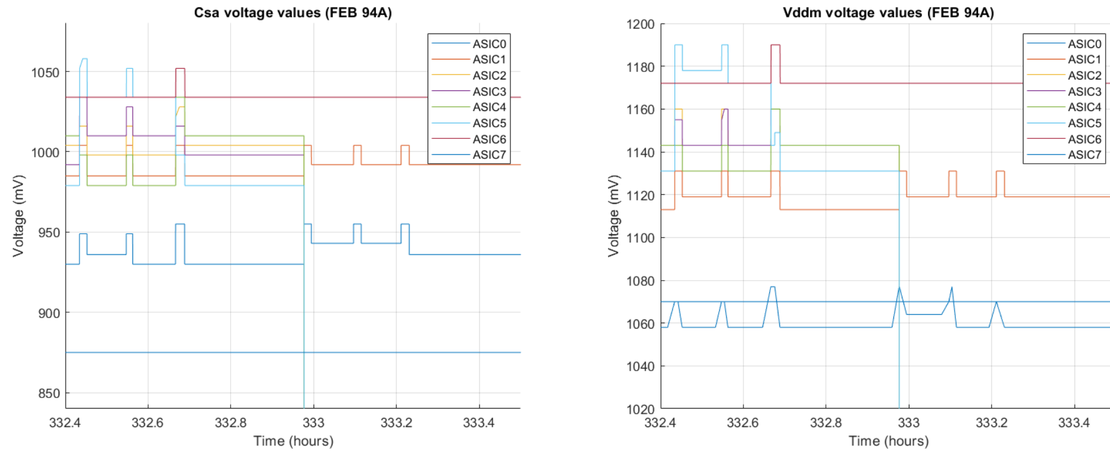

Figure 28: (a) CSA voltage, (b) Vddm voltage

There are two pairs, 1.2V and 1.8V LDOs on each FEB. 1.2V LDOs regulate the voltage for the analog part of the FEB and 1.8V LDOs - the digital part of the FEE. Eight FEBs are arranged into two rows of four ASICs. Each 1.2V analog LDO supplies the power to one row of ASICs. This architecture explains the above-mentioned observations. If one 1.2V analog LDO fails it causes four ASICs to fail, while the failure of two ASICs from the functioning ASICs row was independent of the LDO failure and was observed earlier than the drop in the power supply current reading. The current on the power supply was reduced approx. 50 %, again confirming 1.2V LDO failure.

FEB 94B: Power supply current readings expressed approx. $20 \pm 3\%$ reduction on both FEBs, while no permanent failures have been observed.

FEB 95A: No major failures have been observed after analysing FEB 95A data. After three days into the experiment, a few ASICs started not to respond to the register configurations (approx. $10 \pm 2\%$ missed tests) and showed a decrease in the Vddm voltage values.

FEB 95B: Power supply reading of 1.2V LDO expressed current consumption reduction. Fig. 29 depicts a decay pattern of current consumption for analog LDO.

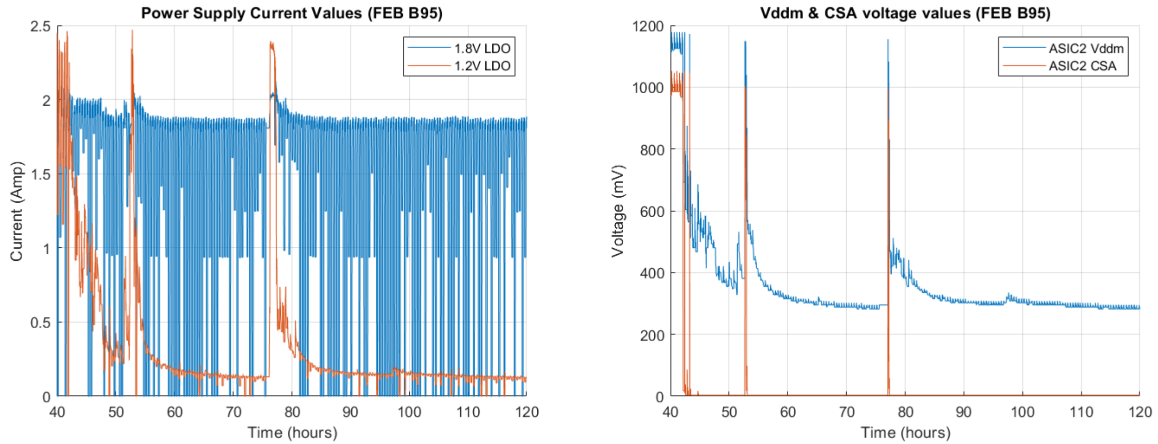

Figure 29: (a) Current consumption of analog and digital LDOs over time, (b) Csa and Vddm voltage values for ASIC2

The decay pattern was distributed over a long time period of approx. 80 hours. At around 76 hours in the experiment, Binder and Lauda were brought back to room temperature to check the connections. Restarting the experiment was followed by successful FEB tests but soon after reaching $-30°C$ decay was preserved, thus suggesting the degradation of the physical characteristics of the 1.2V LDO. Soon after the current was dropped on 1.2V LDO CSA voltage reading on all ASICs dropped accordingly, confirming 1.2V LDO failure according to the FEB schematics.

FEB 96B/97A: FEB 96B and FEB 97A were in a different modifications from the rest. ASICs were substituted by corresponding resistors and LDOs were represented without glob-tops. With this approach, bare LDO functionality was studied. Neither 96 B nor 97 A showed any malfunctions. Results confirmed that bare LDOs without glob top can withstand thermal and electrical tests and previous malfunction origins were diverted either to the electrical stress induced by ASICs or to the thermal stresses induced by the glue covering of LDOs.

FEB135B/136B/138A: FEBs 135B, 136B, and 138A have been examined, as for the last set for the low-temperature power cycling experiment. This set was not cycled before under the Passive/Active cycling experiment. Compared to the previous FEBs tested, the final three showed much fewer malfunctions. As described previously, FEB 135B expressed a drop in current consumption soon after the beginning of the test, see Fig. 30.

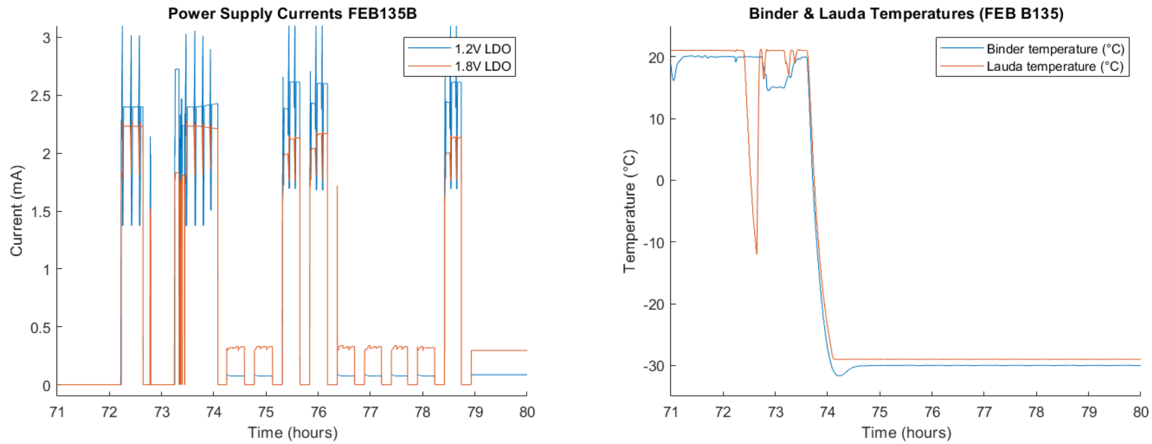

Figure 30: (a) Current consumption of analog and digital LDOs, (b) Binder and Lauda temperature

No permanent failure has been observed by electric and optical tests. Observations made throughout the test, such as a drop of current consumption on 135B LDOs are very similar to the behavior observed before and originate from the LDO performance on low temperatures, though increasing voltage on the power supply did not result in any stability in performance.

ASIC failures Another very important observation made during the experiment is the ASIC connection problem at low temperatures. For all FEBs at least one ASIC was losing the connection with the EMU data readout, though, most of them later passed the electronic tests on the room temperatures. The origins of the above-mentioned problem are not yet fully investigated, possible explanations are to be connected to ASIC's physical properties degrading on low temperatures, data cables, or data readout boards.

3.2.4 Conclusions

Under the scope of the Low-temperature power cycling experiment, a total of eleven FEBs have been tested at a $-30°$C temperature. Every FEB had at least one ASIC not responding throughout the experiment, this effect persisted at low temperatures, but most ASICs have recovered at room temperature. The table 3 summarizes LDO-related failure observations made throughout the experiment.

FEB type	Previous cycling	Cycles Performed	Observed failure cycle	Description
91B	Passive: 150 Active: 100	150	80±5	Current drop 1.8V LDO
93A	Passive: 150 Active: 100	150	5±2	Current drop
94A	Passive: 150 Active: 100	150	75±5	1.2V LDO
94B	Passive: 150 Active: 100	150	-	No failure
95A	Passive: 150 Active: 100	250+	-	No failure
95B	Passive: 150 Active: 100	250+	120±5	Current decay 1.2V LDO
96B (bare LDOs)	Passive: 150 Active: 100	250+	-	No failure
97A (bare LDOs)	Passive: 150 Active: 100	250+	-	No failure
135B	-	100	5±2	Current drop
136B	-	200	-	No failure
138A	-	200	-	No failure

Table 3: LDO-related failure descriptions and their occurrences in the experiment.

Low-temperature thermal cycling provided a better understanding of the STS front-end electronics operation under extensive electrical stress, and freezing temperatures. There were two major categories of failure observations: LDO-related failures and ASIC-related failures.

Temporary ASIC failures were the most common observation, resulting in at least one, and in some (36%) cases, few ASICs not performing tests. More than 70 % of the failing ASICs recovered at room temperature, while the rest of the failures remained permanent.

There were five cases of LDO current reduction or a complete drop. All current reduction patterns were visible on the low temperatures with different occurrences and magnitudes, but post-experimental optical and electronic inspections confirmed only two permanent, FEB 91B and 94A cases. Between two 1.2V and 1.8V LDOs, 1.2V LDO-related cases were more frequent. The more recurring 1.2 V LDO regulator failure can be associated with larger current alterations, leading to more significant temperature differences. One of the most likely causes of LDO regulator failure may be a mismatch between the CTEs[1] of the board's

[1] The coefficient of linear thermal expansion

components. Due to the release of bonds, LDO regulator failure is possible.

Additionally, boards that underwent preliminary active and passive cycling tests were more prone to failure. Furthermore, the FEB without ASICs and glob top on the LDO regulator didn't show any evidence of breakdowns. Different glue materials for glob-tops did not introduce any consistent failure observations.

The electronics in the STS detector will be housing 3,504 1.2V and the same number of 1.8V LDOs. As well as, 14,016 units of STS XYTER ASIC microchips. Low-temperature power cycling results suggest, that due to a large number of FEB units, the risks of malfunctions on STS are very high (though due to low FEB numbers, statistics can not suggest a very precise number). Additional investigation is needed to address the origins of the above-mentioned failures of ASICs. Temporary or permanent failure occurrences gradually increase over time. Operation of the electronics near 0° C temperatures will decrease failure possibilities. To extend the lifespan of the STS detector, narrowing down the number of sudden power cycles is recommended, this can be addressed by gradual, de-ramping shut-off mechanisms to reduce rapid cooling and sudden thermal contractions.

3.3 The STS module temperature-dependent noise tests

The goal of the low-temperature module test is to study the noise dependence on the temperature of the STS modules. The STS module is a very complex device. Performing noise tests on the STS module requires a deep understanding of the components and their schematics. In this thesis only substantial descriptions for the components are provided, for more detailed descriptions and manuals, the following sources can be addressed: [12], [8], [1], [18].

3.3.1 Setup

In this experiment, the cooling setup is very similar to the low-temperature power cycling experiment incorporating Binder, Lauda, and their centralized automated systems. The minor difference comes with the cooling pad which was substituted with a slightly smaller, different design cooling pad to fit the STS module. An additional power supply is used to provide a high - 150V potential difference for the reverse bias regime for the sensor, each positive and negative terminal is supplied with +75V to -75V accordingly. Data readout is handled by the CBM Common readout board (CROB) [20], which is connected to the server with the optical interface. Data cables connecting FEBs and CROB have been shielded and additional ferrites have been mounted to minimize the external noise acquired by the DAQ cables.

Figure 31: STS module mounted inside the frame-holder, connectivity cables, and C-ROB, all inside the climatic chamber - Binder

FEBs are of two kinds, A and B, connecting to the n side and p side of the sensor accordingly. As described in the previous chapters sensor used for the STS is a double-sided silicon strip sensor, with 1024 strips on each, n and p side. FEE (FEB) houses 8 XYTER microchips, each having 128 channels. Fig. 19 represents the schematic design of each channel. Imperfections during the manufacturing process of ASIC as well as the sensor requires each ASIC to be calibrated before the measurements.

3.3.2 Analytical Studies

Analytical studies for the module noise are very important to understand on the one hand possible outcomes of the experiment and on the other hand, evaluate the previously conducted analytical estimations and relate them to the real-life tests. This chapter uses previously discussed analytical studies, and ENC equations 23, 24 to simulate temperature dependence of the noise [12].

Parameters for each noise contributor equations 16, 21 are described below:

1. Parallel current noise (i_n^2)

Parameter	Value
R_{bias}	1.5 MΩ
R_{fb}	20.0 MΩ
I_{det}	4.0 nA
$I_{ESD_{n/p}}$	9.0 nA

2. series voltage noise (e_n^2)

Parameter	Value
R_{Al}	$10.5\ \Omega/cm$
R_{cable}	$0.6M\ \Omega/cm^4$
R_{inter}	4.0 nAΩ
CSA	$\alpha = 0.6, \gamma = 1$
g_m	0.044 A/V

Frequency (1/f) -dependent noise parameters can be addressed experimentally from previous studies, due to the complexity of its analytical evaluation. Contributing parameters for evaluating the total ENC described as an equation 24 are listed below:

Parameter	Value
F_i	0.64
F_v	0.85
F_{vf}	3.41
T_s	$9E^{(-10)}$
A_f	$9.3E^{(-12)}$
C_T	$2.21E^{(-11)}$

Considering the specifications of the module used for the experiment (sensor length - 6 cm, cable length 41 cm) ENC estimations can be made to address the contribution of the above-mentioned parameters, see Fig. 32:

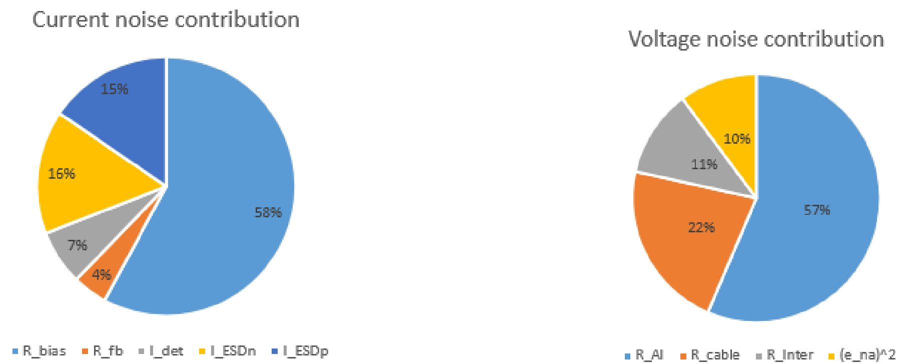

Figure 32: (a) Current noise contribution,
(b) Voltage noise contribution

Finally, using eq. 24 estimated contributors for ENC can be converted to the unit charge and a simulation of total ENC for individual STS module channels dependence over temperature can be generated, see Fig. 32:

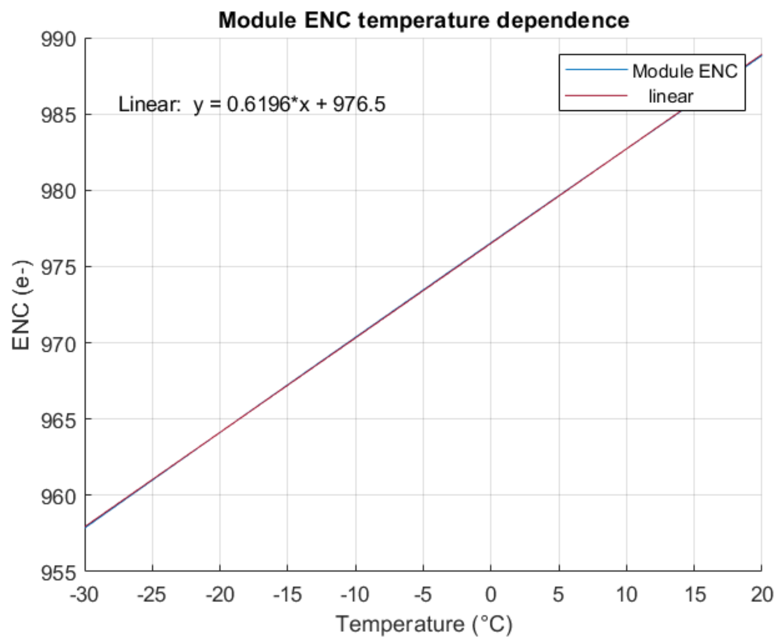

Figure 33: STS module ENC temperature dependence simulation

3.3.3 Current-voltage characteristics

To characterize the sensor saturation current, current dependence on the voltage has been studied. Error in data was relatively high approx. 10%, but this data precision is sufficient to relatively describe the current saturation. The fitting was conducted using Shockley ideal diode eq. 5. The statistical error was approx. 5%. Measurements have been made on two data points, at temperature values 10°C and 20°C. At 20°C the saturation current was measured to be approx. 1 (±5%) μA , while at 10°C current reduced to 0.4 (±5%) μA. Corresponding plots for data and fit functions are depicted in Fig. 34.

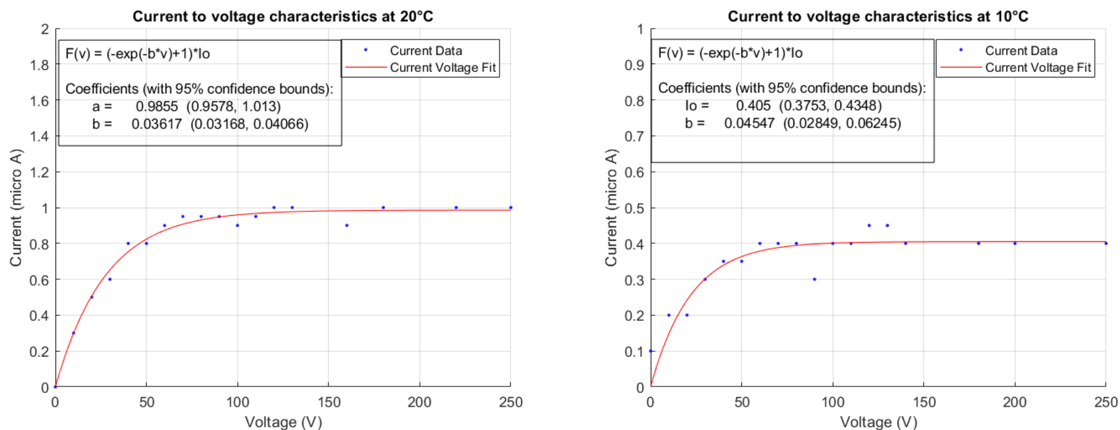

Figure 34: (a) Current-voltage characteristics at 20°C,

(b) Current-voltage characteristics at 10°C

3.3.4 Noise measurement

The noise measurement relies on the output function of the ASIC channel's discriminator. From the s-curve scan, the noise measurements are obtained. On the CSA portion of each channel, different amplitude pulses are introduced. The discriminator response to the injected pulses should ideally be a step function, but the measurement function is smeared due to noise in the system. The discriminator responses are fitted with an error function $erfc(\frac{x-\mu}{\sqrt{2}\sigma})$, where the function's width is the noise measurement of the noise amplitude and the function's mean value represents the discriminator threshold. In every channel, the An analog-to-digital converter (ADC) noise levels are determined by averaging the contributions of all discriminators. Since a valid hit is only generated when the lowest ADC threshold is exceeded, the effective system noise can be estimated by considering only the contribution of the first discriminator, a more detailed description of noise measurement can be accessed in the following source [12].

In the scope of the experiment, the temperature dependence of module noise had to be characterized. For each FEB (A and B) and their ASICs (each FEB contains eight XYTER V2.2 microchips), noise measurement tests were required in order to attain the noise and supplementary data from the module per measurement.

The same temperature range as the previous Low-temperature power cycling tests has been selected. From 20° C to −30° C in 10-degree decrements, Summing up (8 ASICS X 2 FEBs X 6 temperature points) 96 total measurements for ENC, ADC gain, and ADC threshold, altogether 288 plots.

Equivalent noise charge (ENC) is the total charge contributed by the noise in the system measured in elementary charge units.

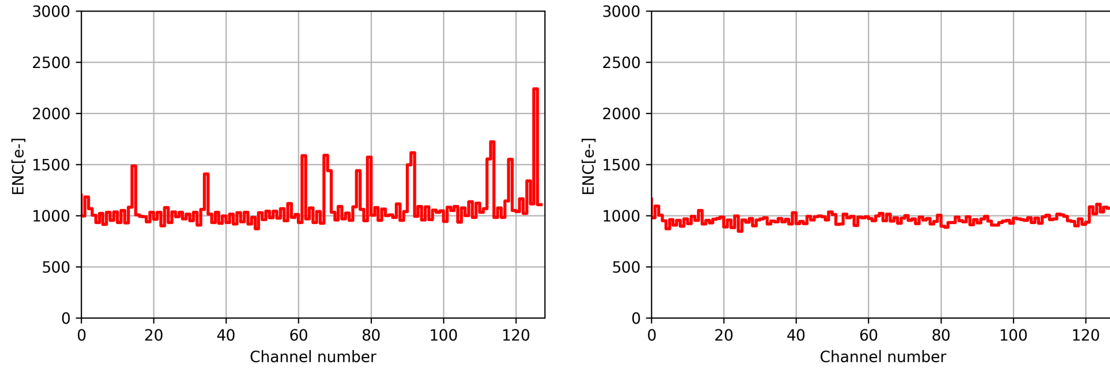

Figure 35: (a) Error function width for each channel - noise amplitude for FEB 73B (p side) ASIC 5, (b) Error function width for each channel - noise amplitude for FEB 72A (n side) ASIC 5

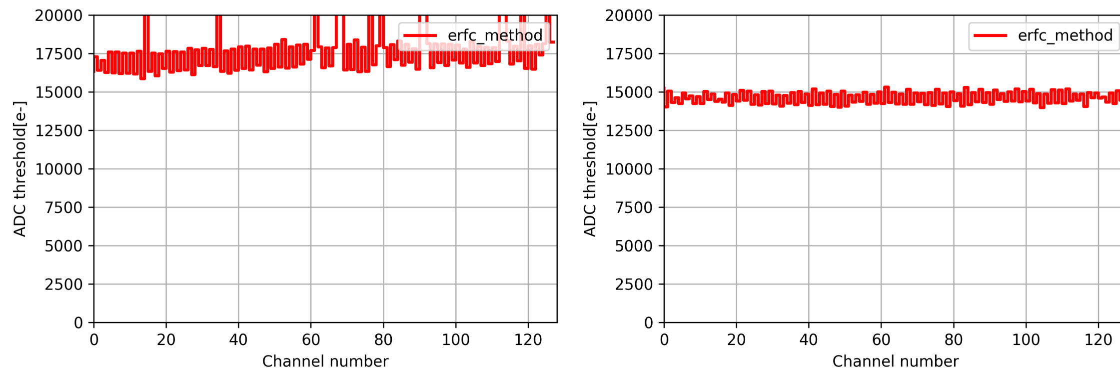

Figure 36: (a) Mean value - ADC threshold for FEB 73B (p side) ASIC 5,
(b) Mean value - ADC threshold for FEB 72A (n side) ASIC 5

The ENC measurements have been made for every 128 channels of every ASIC, an example of the corresponding data plot can be seen in Fig. 35 (a) p side and (b) n side. The fluctuation of the data was relatively higher for the p side. Some channels expressed considerably higher deviations from the mean value, i.e. Fig. 35 (a) channel 62. This pattern was repeated on the threshold measurements, relatively higher for the p side. Channels expressing greater deviation remained the same. These results indicate that some channels expressed considerably higher reading values than others. Fig. 37 depicts ADC gain values for each channel. Deviations in these values correlate with the observations above, once again supporting the above-mentioned suggestion about "faulty" channels.

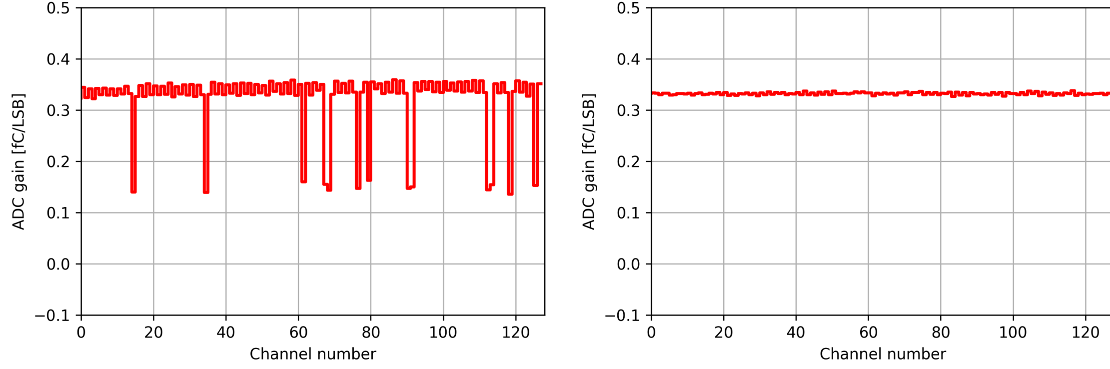

Figure 37: (a) Channel ADC gain values for FEB 73B (p side) ASIC 5,
(b) Channel ADC gain values for FEB 72A (n side) ASIC 5

Combined ENC plots were generated in order to analyze the data from every ASIC, as has already been mentioned, for every ASIC there are 128 channels, each providing ENC information, and there are two FEBs for the sensor sides n and p, therefore combined ENC plots will have n and p information distributed on 1024 channels. There were preliminary tests performed on the module, which identified faulty ASICs, in the following plots statistics from those ASICs will be neglected to avoid inconsistencies. ASICs excluded from the n side: 0, 1, 4; p side - 0. With the previous studies, it is possible to analyze the noise data and relate it with the faulty components: sensor, cable, or ASIC [12]. Component-specific malfunctions can be identified as significant drops in the noise measurement. The furthermost component from the DAQ is the sensor, therefore, the sensor channel malfunction is only observed if the corresponding ASIC and micro cables are functioning correctly, the similar approach can be used for the faulty cables and ASICs. The first significant drop relates to the sensor's faulty channel, the second to the cable, and the final to the ASIC channel. The full ENC measurements, component-corresponding thresholds, as well as faulty channels, are listed in the appendix. ENC measurements at 20° C and at $-30°$ C are depicted in Figures 38 and 39.

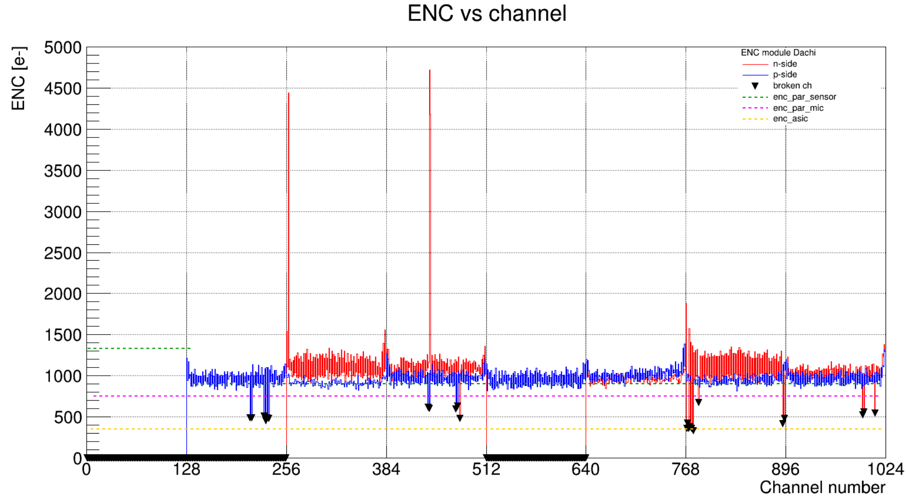

Figure 38: ENC measurement at 20° C per channel for every ASIC

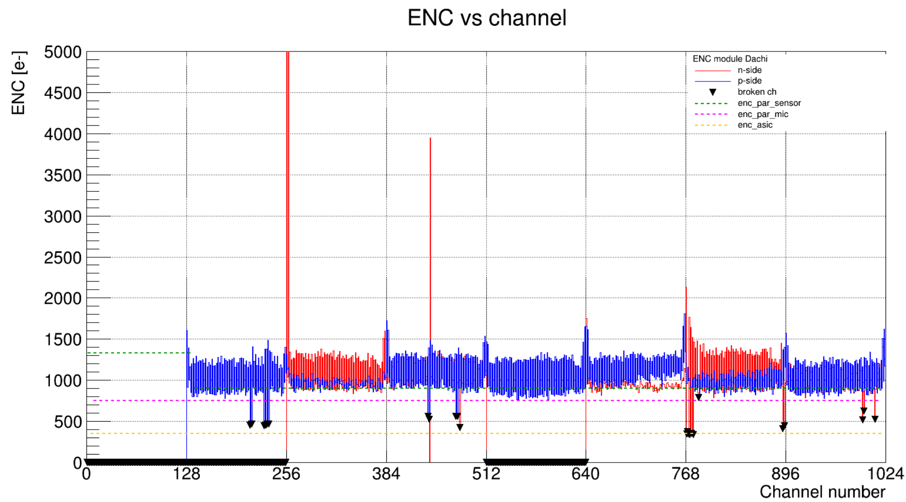

Figure 39: ENC measurement at −30° C per channel for every ASIC

There was no significant difference observed in the broken channel statistics between 20° C and −30° C. Only one ASIC channel difference was observed at −30° C compared to the 20° statistics. The total number of faulty channels did not exceed 10. Statistics about the malfunctioning channels can be observed in Fig. 40, on the leftmost columns values are increased due to disabled ASICs (three ASICs on the n side and one ASIC on the p side).

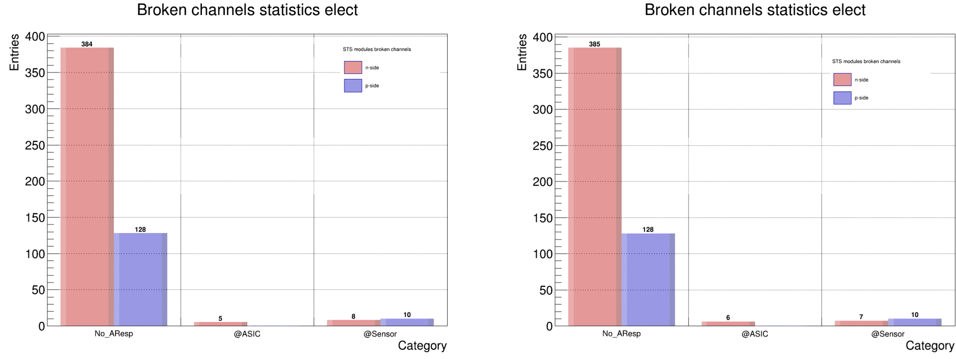

Figure 40: (a) Broken channel statistics at 20° C, (b) Broken channel statistics at −30° C

Calibration of ADC with error function fits has identified corresponding ADC thresholds. Threshold levels for temperature values 20°C and −30°C can be seen in Fig.

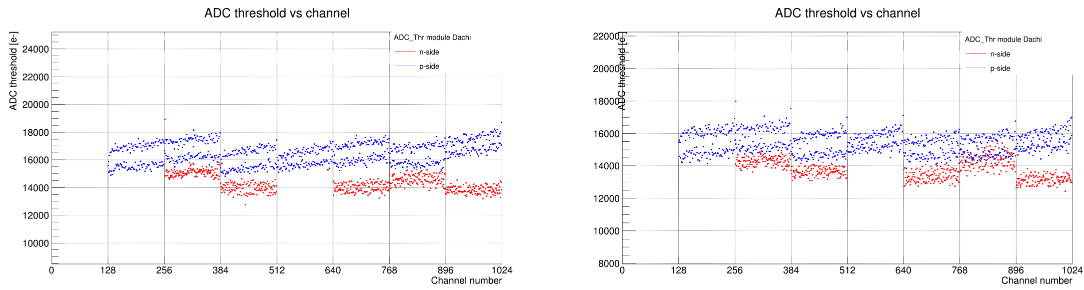

Figure 41: (a) ADC thresholds per channel at 20° C, (b) ADC thresholds per channel at −30° C

ENC data can be used to generate the ENC distribution. During the analysis process differences between odd and even channels have been observed. These observations have been consistent with the previous noise studies [12] [5]. In the following plots, odd and even channels are marked with different colors. Plots for all temperatures steps are shown in Appendix, below are listed measurements for 20°C and −30°C, see Figures 42, 43.

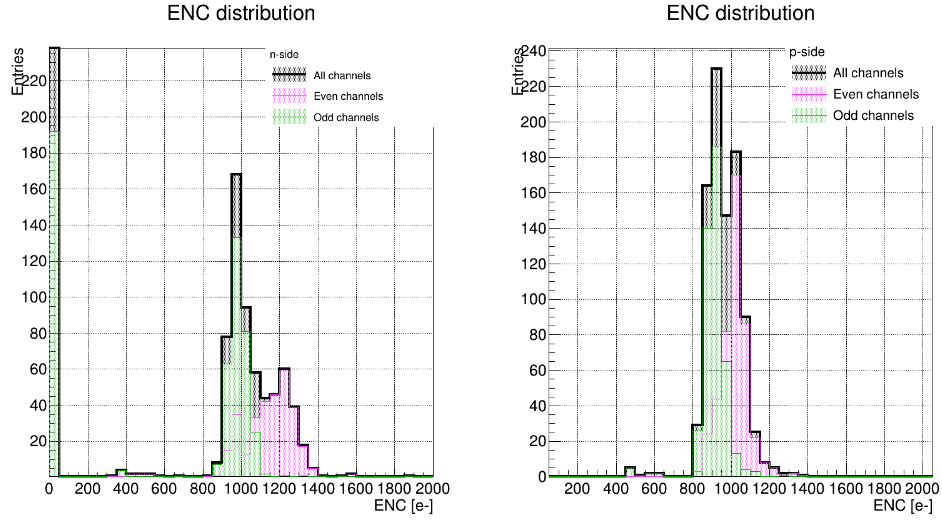

Figure 42: ENC distribution at 20° C

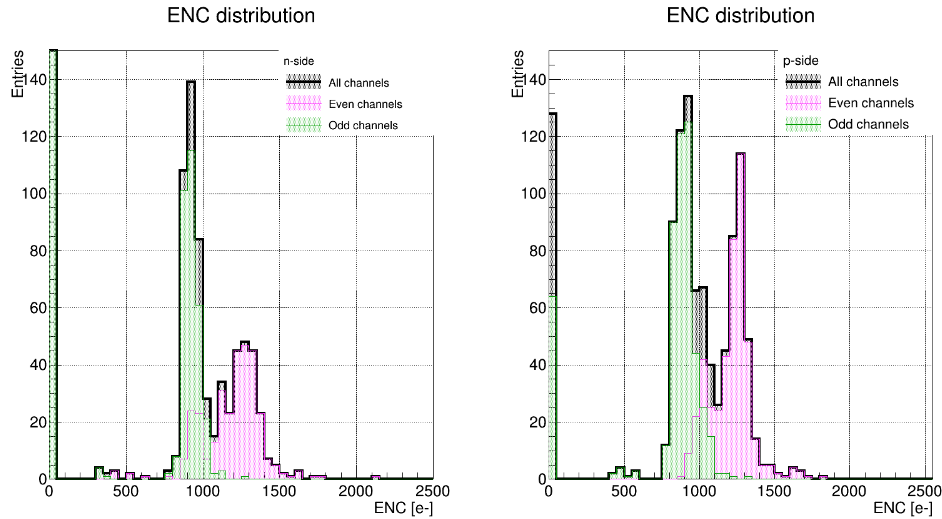

Figure 43: ENC distribution at $-30°$ C

Differences in the odd and even channels for both sides of the sensor have been consistent on all temperatures. An explanation of this phenomenon can be related to the design of the module itself. Every XYTER microchip is connected to the sensor with two arrays of micro cables. One housing odd channels and the other, even channels only. Considering these differences, further analysis of the noise studies is performed separately for odd and even channels.

For every temperature values four different plots were generated, corresponding sensor sides n and p, with odd and even channels separated. To identify the ENC values characterizing the noise on the specific

temperature point ENC distribution data has been fitted with the Gauss distribution function. Detailed information about the analysis and plots for every temperature point is presented in the Appendix, only two temperature point plots are depicted in this chapter.

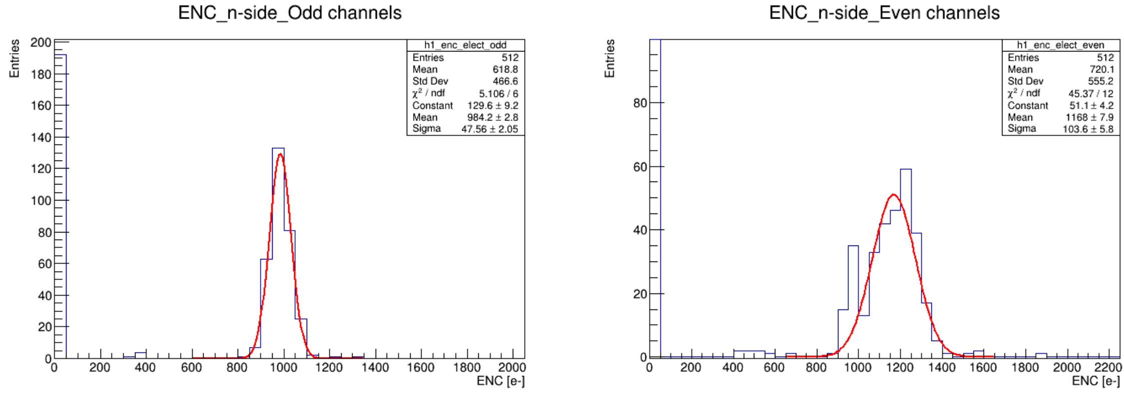

Figure 44: Gauss function fit for n-side at 20° C, (a) odd channels, (b) even channels

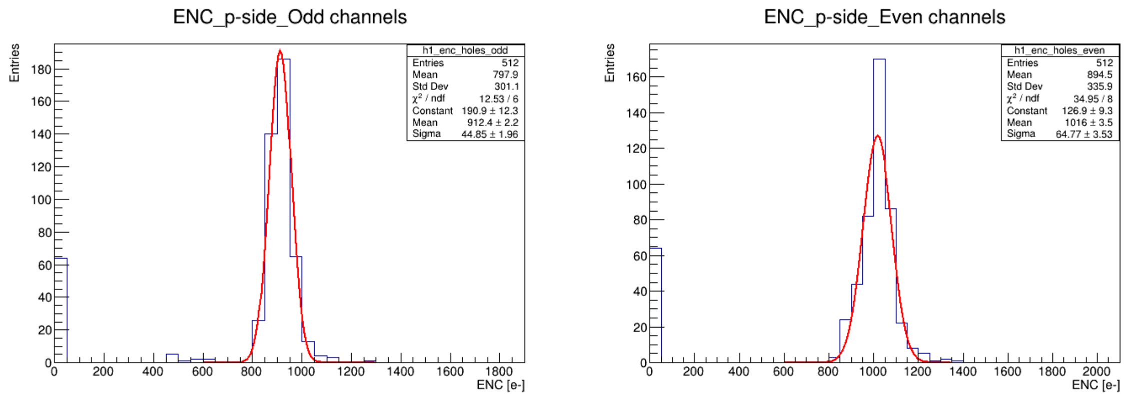

Figure 45: Gauss function fit for p-side at 20° C, (a) odd channels, (b) even channels

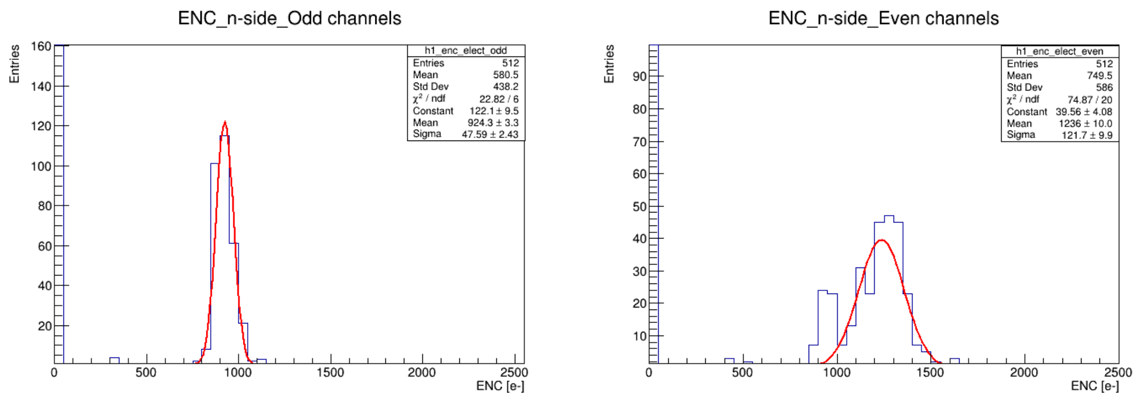

Figure 46: Gauss function fit for n-side at −30° C, (a) odd channels, (b) even channels

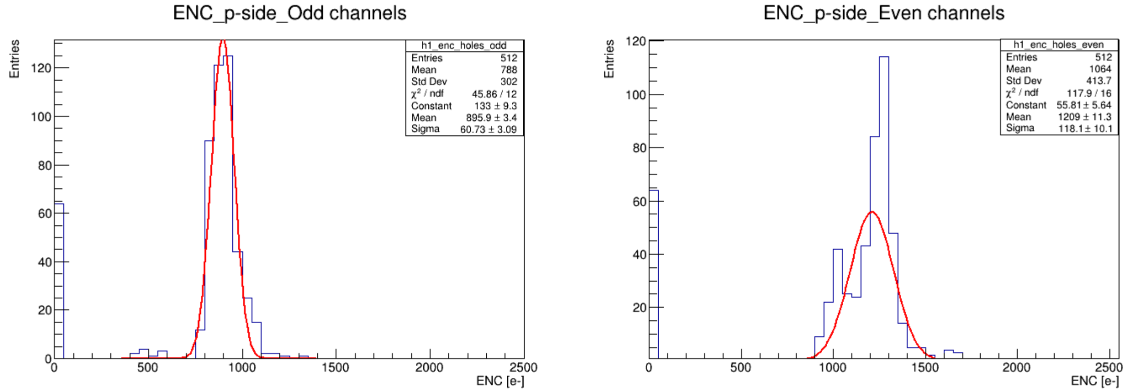

Figure 47: Gauss function fit for p-side at $-30°$ C, (a) odd channels, (b) even channels

The mean value ENC distributions over six temperature values for both n and p sides and corresponding odd and even channels have been evaluated. The following plots depict ENC mean value dependence on temperature and their corresponding linear fits, Fig. 48.

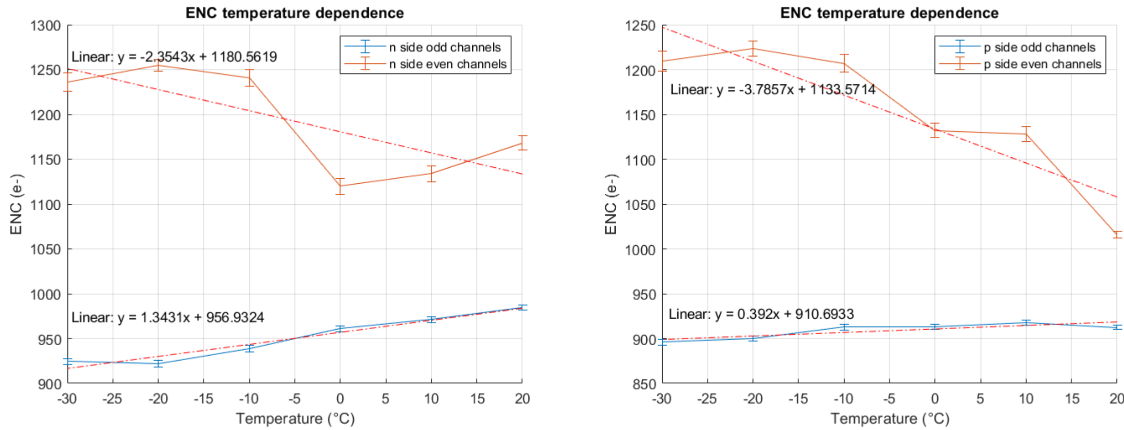

Figure 48: (a) n side ENC temperature dependence, (b) p side ENC temperature dependence

Sigma values for Gauss function fits describe the standard deviation of the data. Sigma dependence on the temperature has been analyzed in order to understand the statistical characteristics of the ENC data, Fig. 49.

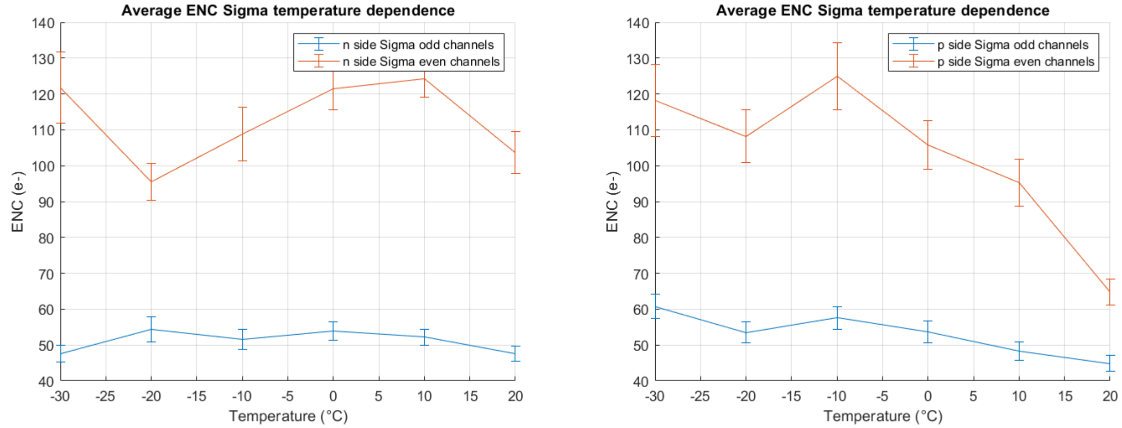

Figure 49: (a) Temperature dependence of standard deviation of the averaged ENC data for n side, (b) Temperature dependence of standard deviation of the averaged ENC data for p side temperature dependence

3.3.5 Conclusions

In order to characterize the sensor used for the experiment current-voltage diagrams have been generated by the corresponding data. There were two temperature values on which the characteristics have been evaluated, at 20°C, and at 10°C. The measurements suggested saturation leakage currents on these temperatures under a reverse bias regime. Saturated leakage current at 20°C measuring $\approx 1\mu$A, reduced by 60% at 10°C.

There were obvious differences between odd and even channel measurements. Differences in observations, with odd and even data values have been seen in previously conducted experiments [12]. Therefore, this can not be directly related to the current experimental setup. ASIC remains one of the greatest contributors to the noise. XYTER chips furthermore require a great amount of current mainly, for powering CSAs separated in two paths of a digital-to-analog converter (DAC), biasing selectively specific set of channels, used to operate other CBM experiment systems - MUCH see Fig. 2. DACs used to bias are placed at one edge of the ASIC, in the area with the higher channels numbers. Though, the filtering design of odd and even channels is different, i.e. even channel current is being filtered at DAC, while odd channel current is filtered after biasing CSAs [12]. There is a difference in the micro cabling design. Each ASIC is attached to the sensor with a set of double micro cables for even and odd channels. On the working STS detector, modules will be attached to the carbon fiber ladders, with all components fixed precisely in place. The microscopic fixation ensures all cables are stretched across the ladder with no curvature. The structure of the module frame in the current experiment did not replicate the design of the carbon-fiber ladders, due to technical constraints. This design resulted in a curvature in the micro cables layout. Micro cables are shielded from external influence with screening tape. There have not been any deeper studies conducted in the scope of this work to address this matter, but it is plausible, that due to the change in design as well as the location of the micro cables in relation to the frame and cable shielding, cables experienced different contributions of

external noise. Cabling design in combination with above mentioned, ASIC-related differences between odd and even channels can be correlated with the origins of the differences in the ENC measurements between odd and even channels.

Analytical estimations of the ENC temperature dependence suggested ENC value very close to what has been observed on odd channels during the experiments, with only $\approx 2\%$ error for n side and $\approx 7\%$ error for the p side odd channels at 0°C. Somehow, ENC mean values for even channels expressed much greater deviations form the analytical estimation. N side even channels had $\approx 20\%$ error and p side even channels expressed $\approx 16\%$ offset.

The slope value for linear function fit resulted in $m \approx 0.6$ (ENC/T). Odd and even channel fit functions delivered very different slopes. ENC temperature dependence simulation (Fig. 33) generated by analytical equations 24, and ENC mean value linear fits (Fig. 48), resulted following slopes:

Data type	Value (ENC/T)
Simulated	0.6
n side odd	1.34 ± 0.05
n side even	-2.35 ± 0.05
p side odd	0.39 ± 0.05
p side even	-3.78 ± 0.05

Standard deviations had a tendency to increase as the temperature decreased, mainly for the p-side of the sensor, while n-side measurements were more dispersed without any obvious pattern. It is clear from the measurements that both odd and even channels have additional contributors to noise, other than what was considered by the simulation. The origins can be related, to the above-mentioned differences in ASIC, cabling design, and possibly different exposure to external sources. Needs to be mentioned, that other ongoing noise projects suggested that the operation of the Binder, which uses an electrical pump, had an influence on ENC measurement as the temperature for their modules remained constant at room temperature. Pump's operational power increases as the temperature decreases, it is plausible that ENC measurements will have a significant contribution from this source as the temperature reaches very low values. Arrangement of the shielding, odd and even channel micro cables can also be generating different exposure levels to the external sources. The sensor is very sensitive to EM waves, and therefore to visible light. It has been covered with a plastic holder and the Binder widow has been covered with black cloth, though a minor contribution from light is still possible.

A possible upgrade to the experiment would be to generate ENC measurements at low temperatures without having the influence of the other external electrical devices, though it is a hard task. Binder loses the $-30°C$ temperature very soon as the pump is turned off and electronics heat up rapidly. One way to address this challenge would be to build a custom electrically shielded chamber with liquid cooling supplied externally.

To conclude, the STS module noise tests confirmed the previously observed differences between odd and even

channel noise measurements. Experiment results were in the same order of analytical estimations, and odd channels followed the analytically expected pattern of temperature dependence. While even channels resulted in higher deviations from the simulation and a negative slope of the ENC data. For the STS operation in the CBM experiment, it suggested having odd and even channels recalibrated separately for acquiring consistent measurements. Varying temperatures will result in changes in the measurements for odd and even channels, therefore module behaviors on different temperatures need to be studied and understood in more detail. For the stable performance of the STS modules it is recommended to maintain a constant temperature, with well-understood noise dependencies.

4 Summary

Master's work, Characterization of Compressed Baryonic Matter (CBM) Silicon Tracking Systems (STS) detector modules is a contribution to the creation of the STS detector in FAIR experiment under GSI collaboration at FAIR facility in Darmstadt, Germany. The thesis covers two experiments: Low-temperature power cycling and The STS module temperature-dependent noise tests, conducted on the fundamental structural components, the STS module and FEBs of the STS detector.

A large amount of power dissipated on the STS detector and radiation environment requires intensive cooling of the systems. In the scope of Low-temperature power cycling tests, eleven electronic boards, responsible for the functionality of the STS detector, underwent extensive electrical and thermal tests. The goal was to examine the operational thresholds of the electronics and identify possible failure sources. The tests identified two distinct origins of the failures, one being connected with the Low-dropout voltage regulator (LDO), mainly with analog, and others with XYTER microchips. Lower temperatures resulted in an increased frequency of failures in both ASIC and LDO components, as occurrences drastically increased after a few hundred power cycles. As a result, experiments showed that electronics are prone to frequent failures at $-30°C$, suggesting minimizing the unnecessary power cycles on electronics, while operating the STS and maintaining the temperatures as stable as possible on relatively warmer levels.

The STS module is the essential fundamental component of the STS detector. The STS detector is a pyramid-like structure with, an eight-layer array of modules. Modules are responsible for acquiring crucial data for the CBM experiment, on the fundamental particles generated after collisions of the accelerator beam to the target. The STS module consists of three components, a silicon sensor, micro cables, and electronic boards. Under the scope of the experiment, noise measurements at different temperatures have been made. Sensor-specific, physical characterization, such as current-voltage analysis has been performed. The tests confirmed the correlation of simulated analytical estimations with the experimental measurements. Noise to temperature dependencies has been studied in $20°C$ to $-30°C$ temperature range. Tests identified differences between odd and even channels, for both p and n sides of the silicon strip sensor, with odd channels matching analytical estimations with high precision, in contrast with even channels having more than 15 % deviation from expected. In conclusion, it is suggested to have different calibrations separately for odd and even channels, though a better understanding of the temperature-related behavior of the module is suggested before making the STS detector operational in the CBM experiment.

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5 Appendix

5.1 ENC plots with temperature variations

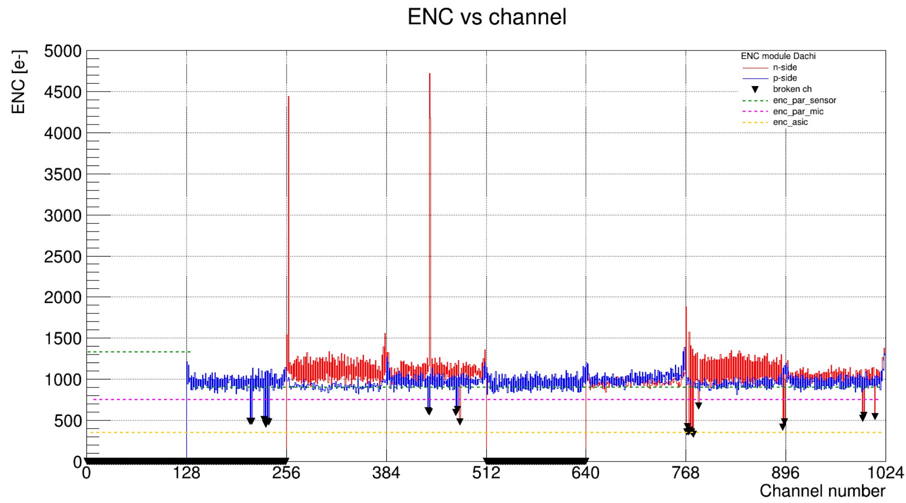

Figure 50: ENC measurement at 20° C

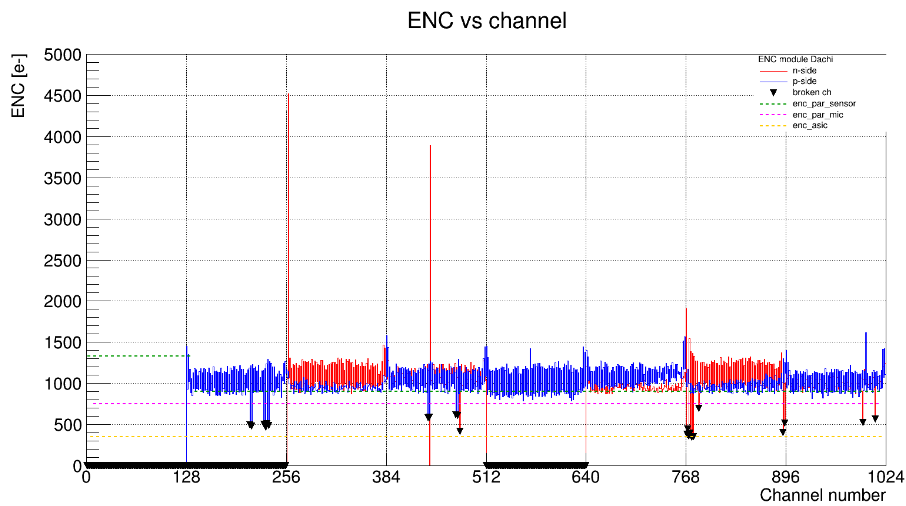

Figure 51: ENC measurement at 10° C

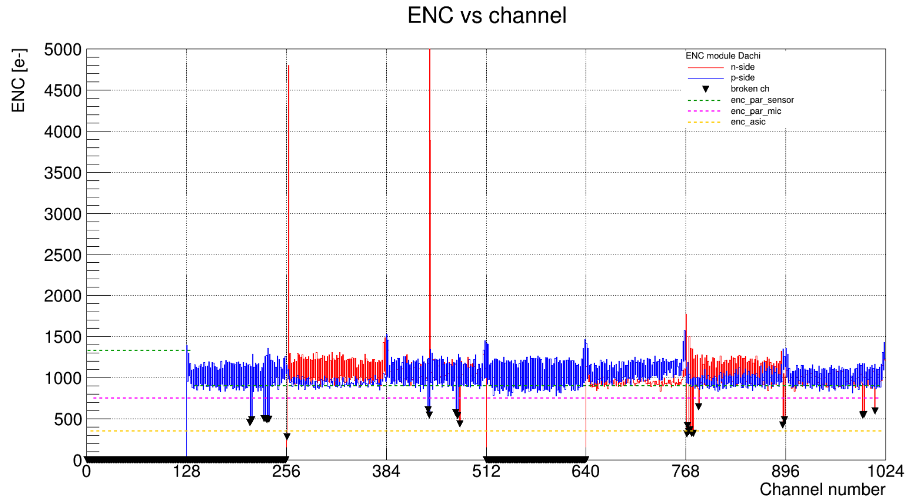

Figure 52: ENC measurement at 0° C

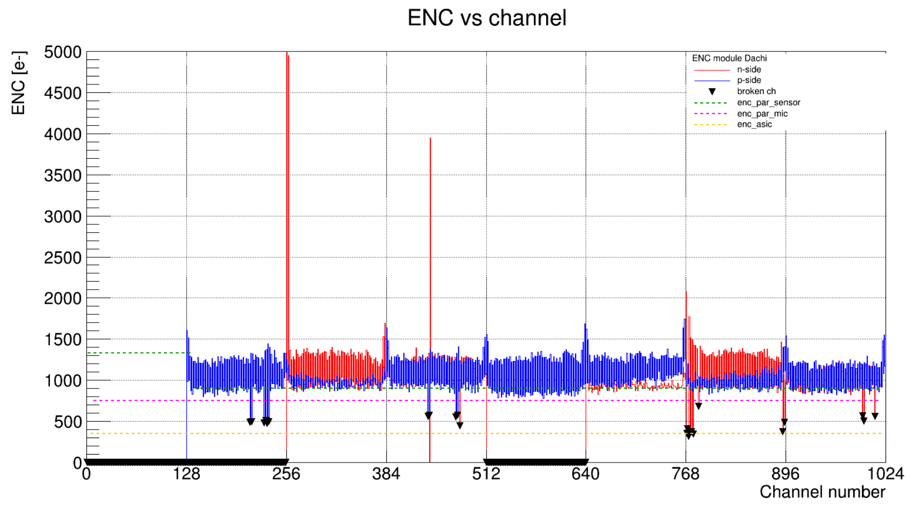

Figure 53: ENC measurement at −10° C

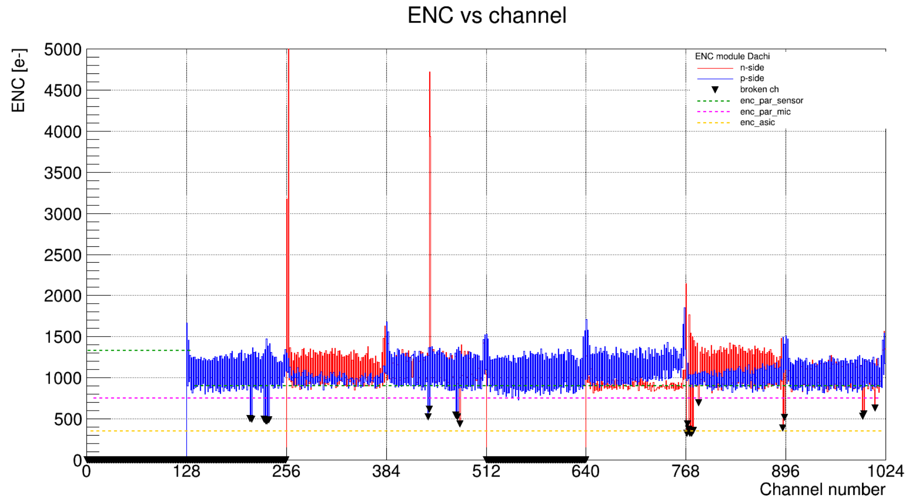

Figure 54: ENC measurement at $-20°$ C

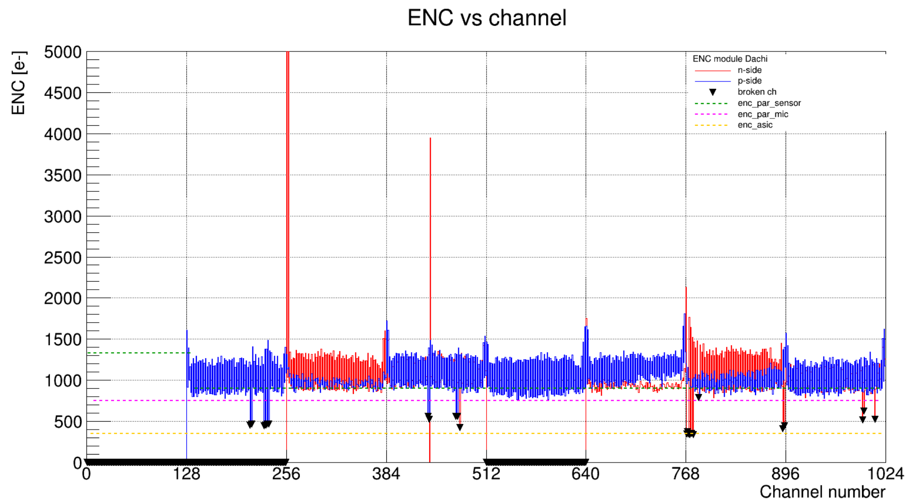

Figure 55: ENC measurement at $-30°$ C

5.2 ENC distribution plots

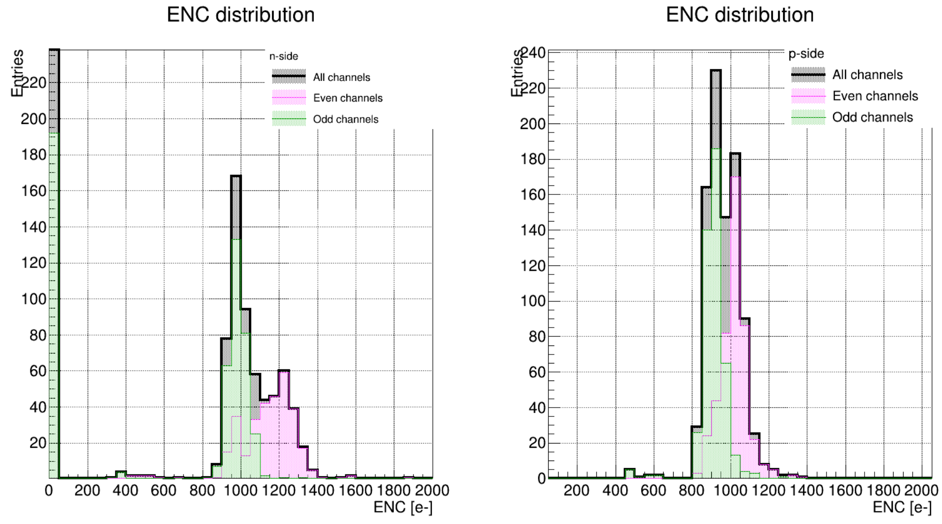

Figure 56: ENC distribution at 20° C

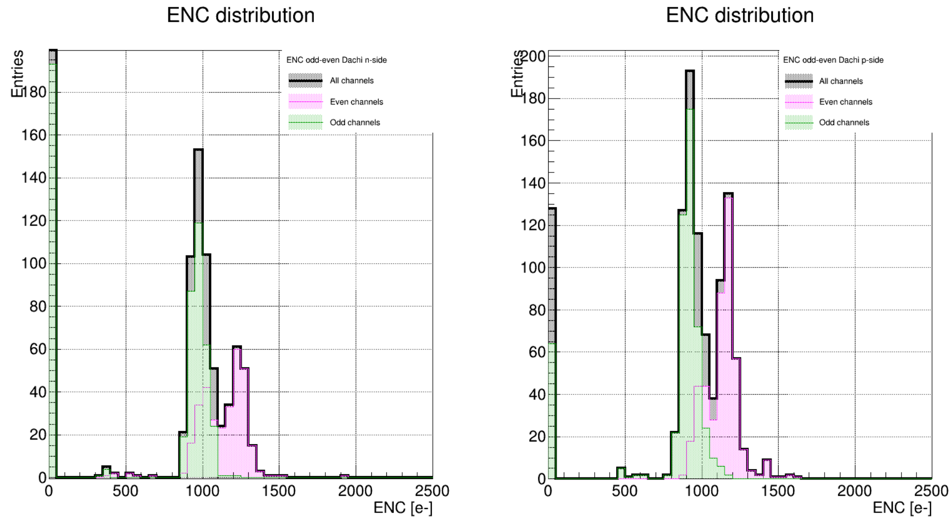

Figure 57: ENC distribution at 10° C

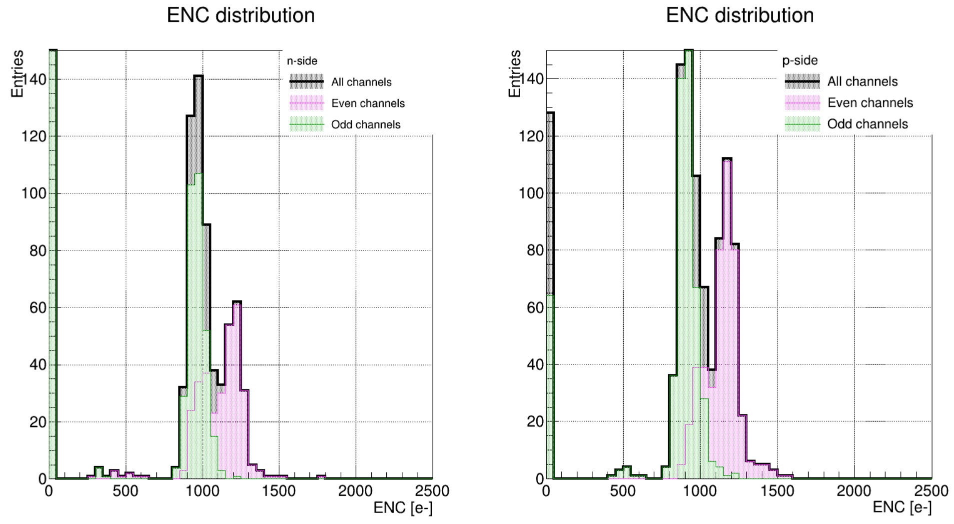

Figure 58: ENC distribution at 0° C

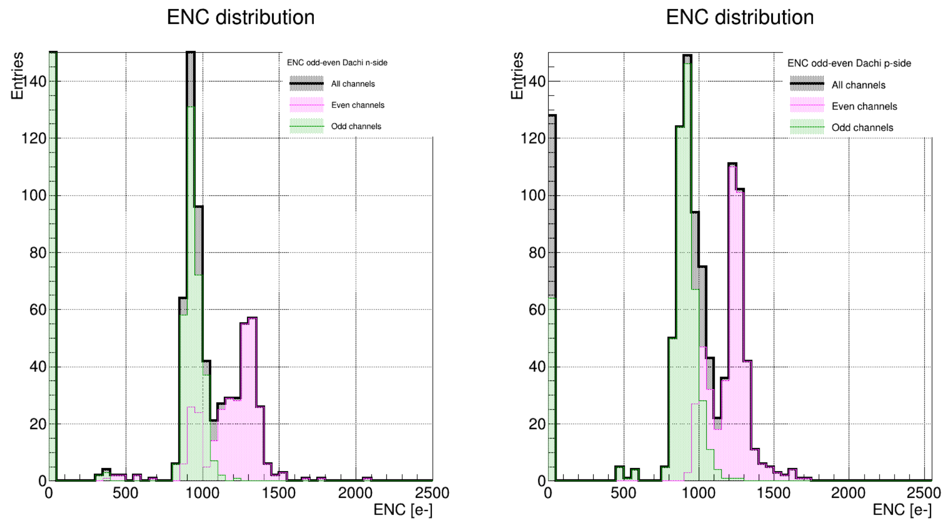

Figure 59: ENC distribution at $-10°$ C

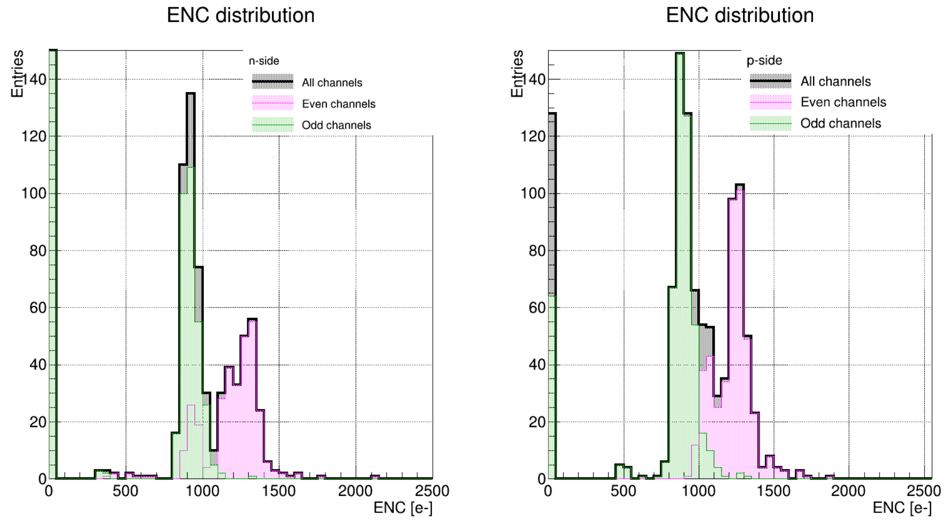

Figure 60: ENC distribution at $-20°$ C

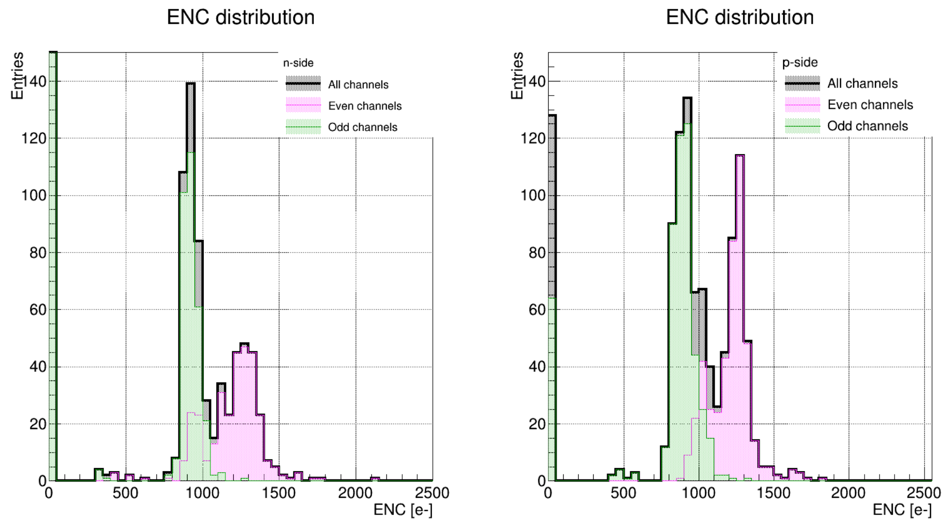

Figure 61: ENC distribution at $-30°$ C

5.3 ENC distribution Gauss fits

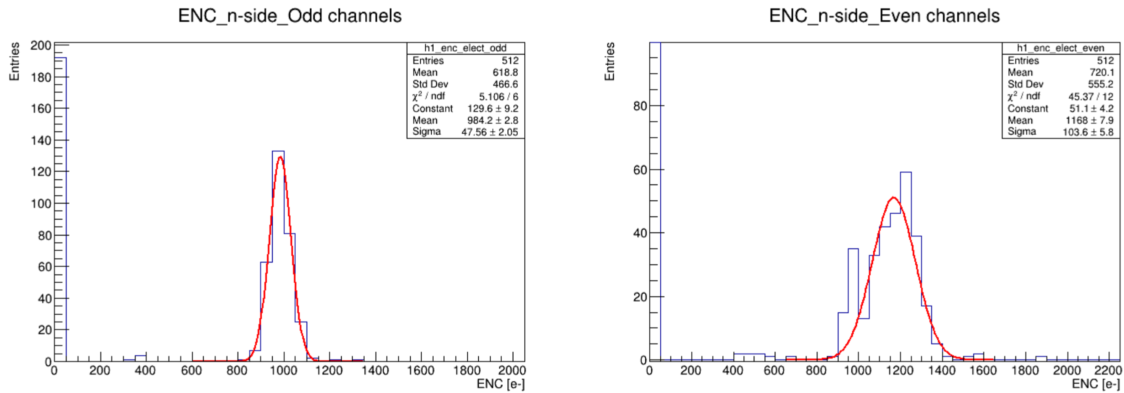

Figure 62: Gauss function fit for n-side at 20° C, (a) odd channels, (b) even channels

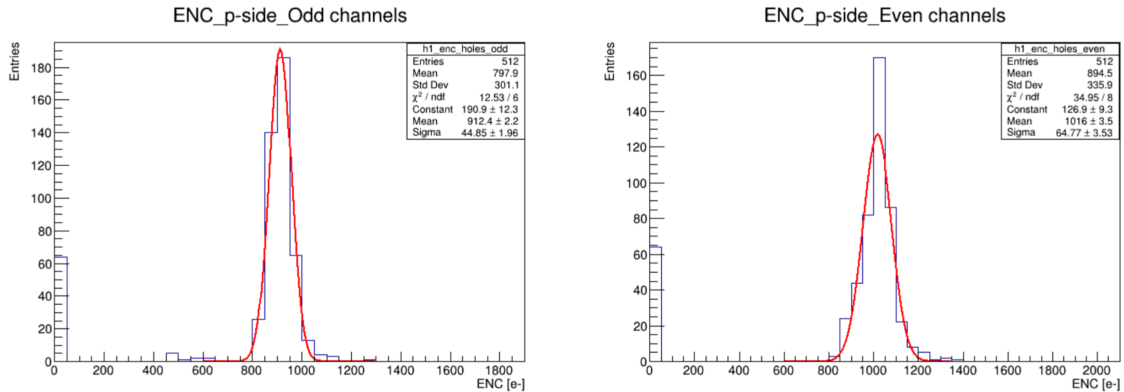

Figure 63: Gauss function fit for p-side at 20° C, (a) odd channels, (b) even channels

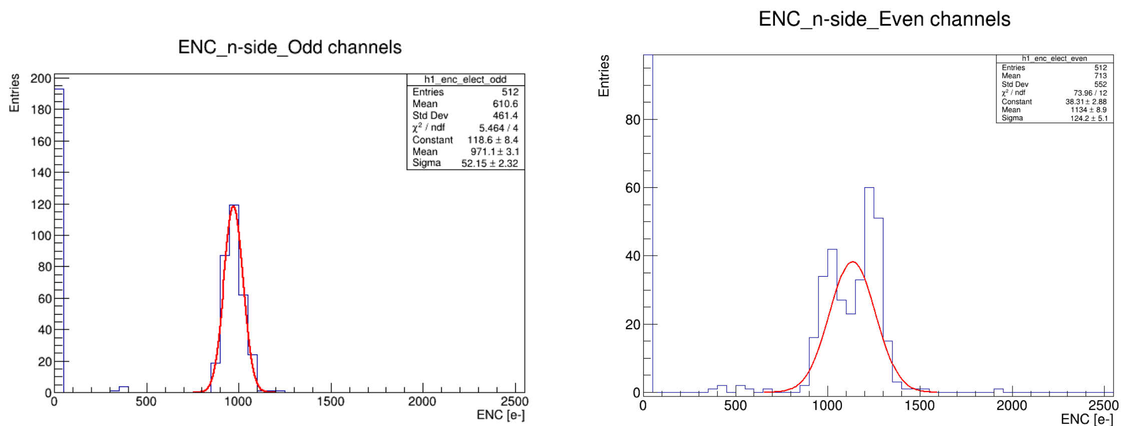

Figure 64: Gauss function fit for n-side at 10° C, (a) odd channels, (b) even channels

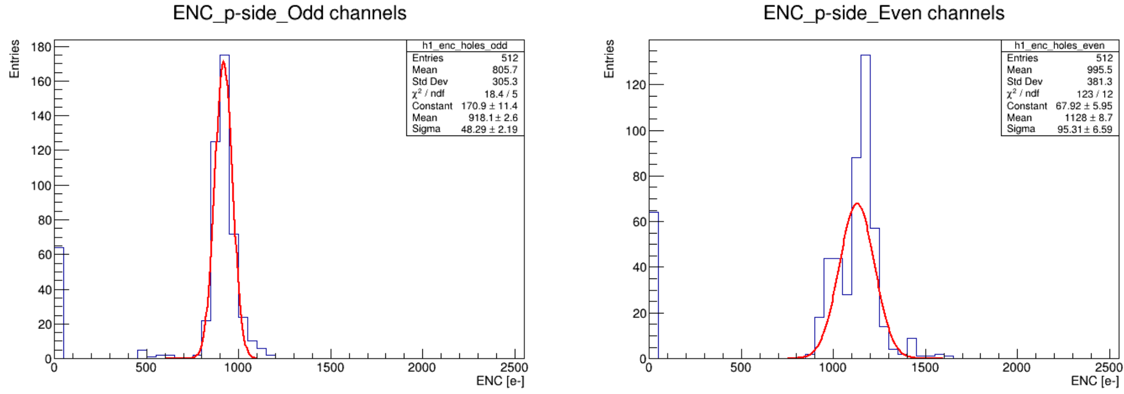

Figure 65: Gauss function fit for p-side at 10° C, (a) odd channels, (b) even channels

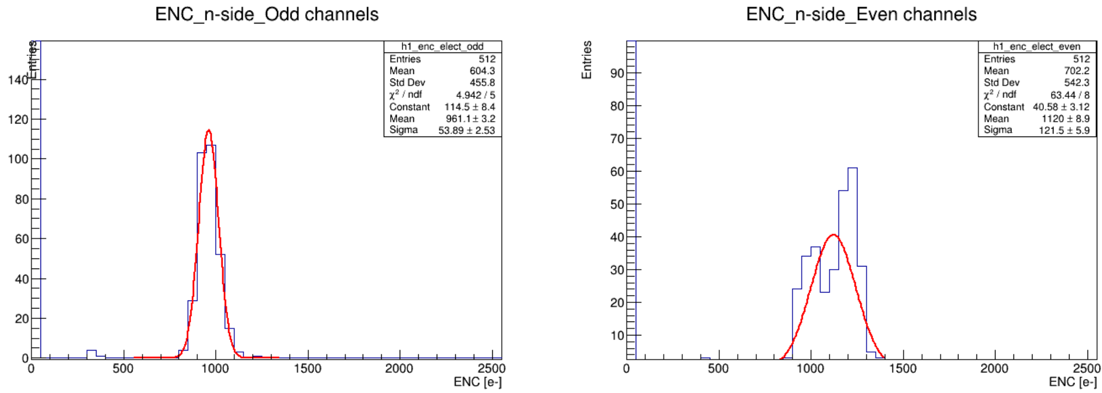

Figure 66: Gauss function fit for n-side at 0° C, (a) odd channels, (b) even channels

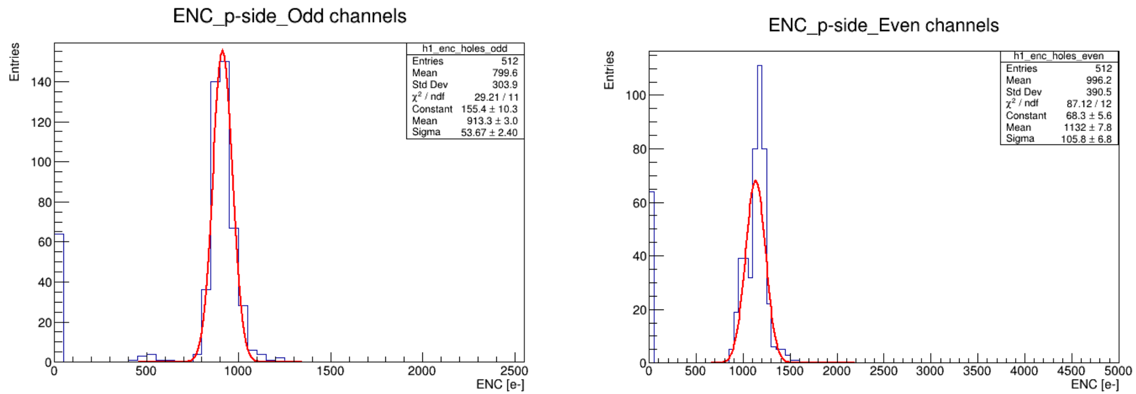

Figure 67: Gauss function fit for p-side at 0° C, (a) odd channels, (b) even channels

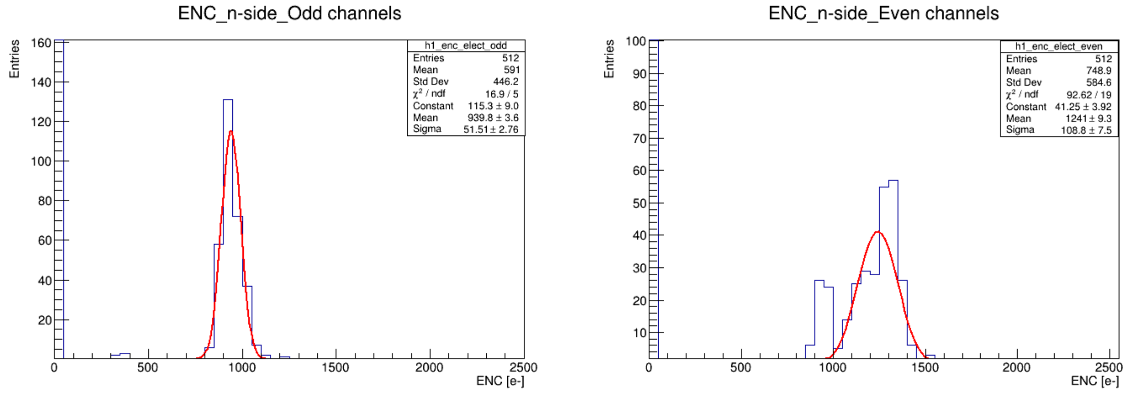

Figure 68: Gauss function fit for n-side at -10° C, (a) odd channels, (b) even channels

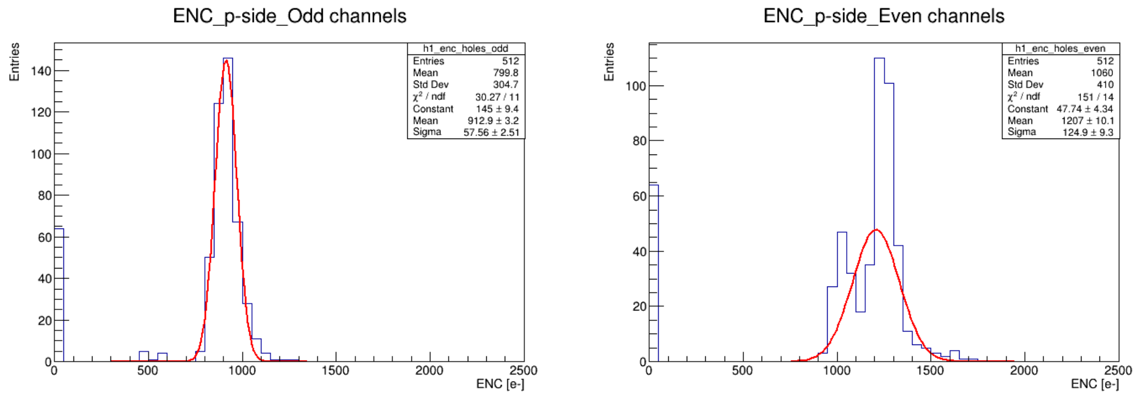

Figure 69: Gauss function fit for p-side at -10° C, (a) odd channels, (b) even channels

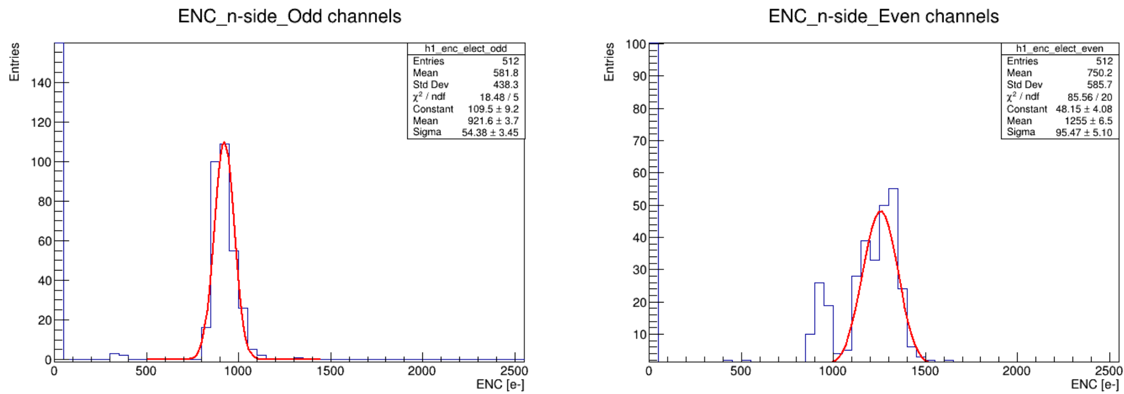

Figure 70: Gauss function fit for n-side at -20° C, (a) odd channels, (b) even channels

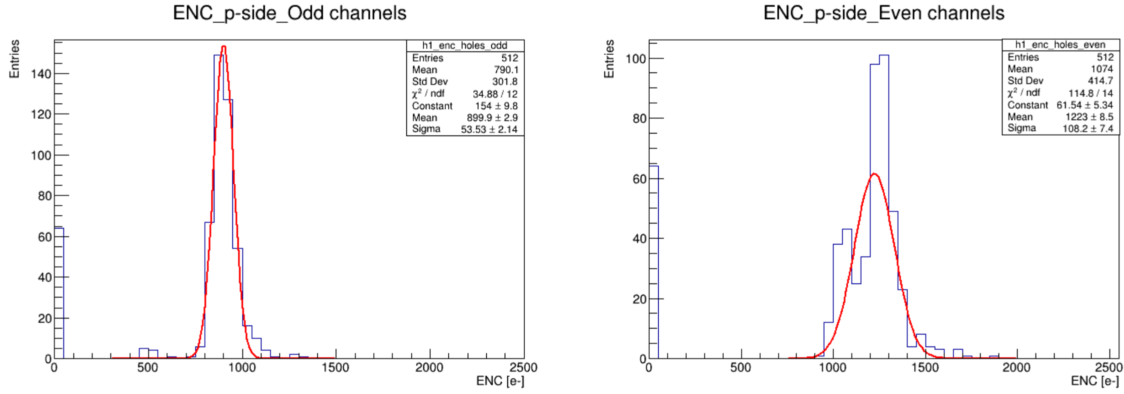

Figure 71: Gauss function fit for p-side at $-20°$ C, (a) odd channels, (b) even channels

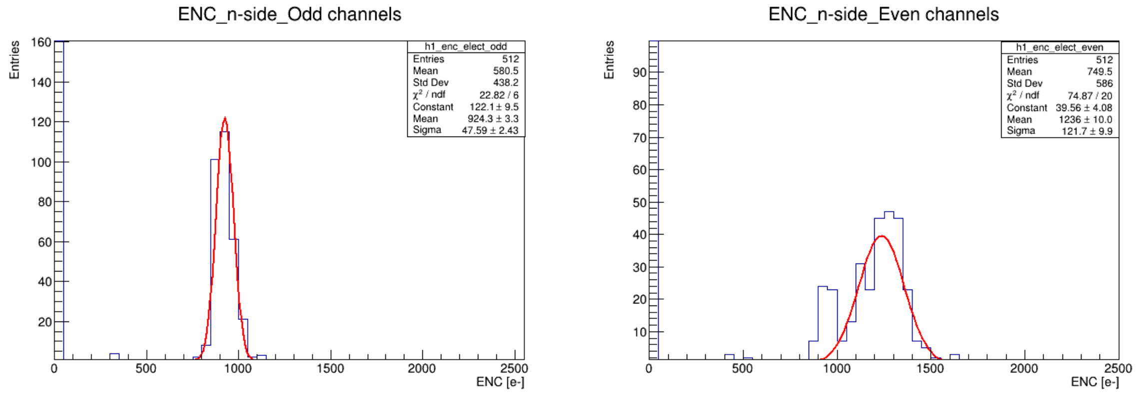

Figure 72: Gauss function fit for n-side at $-30°$ C, (a) odd channels, (b) even channels

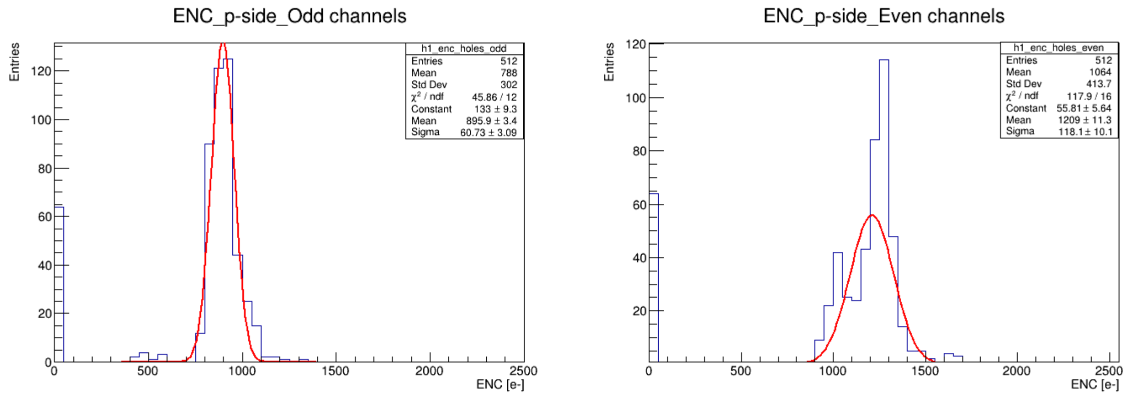

Figure 73: Gauss function fit for p-side at $-30°$ C, (a) odd channels, (b) even channels